ACTA IMEKO
February 2015, Volume 4, Number 1, 19 – 25
www.imeko.org

Development, implementation and characterization of a DSP based data acquisition system with on-board processing

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ABSTRACT
This paper presents the development, implementation and characterization of a data acquisition (DAQ) system capable of on-board processing the acquired data. The system features four differential channels, with 1 MHz bandwidth, simultaneous acquisition, 9 independent bipolar ranges, and a maximum sampling rate of 600 kS/s. The analog DAQ inputs are protected against incorrect connections even direct connection to the power grid voltage. This protection ensures that the DAQ can recover to full operation without the need to replace any damaged components or fuses. A 450 MHz SHARC digital signal processor (ADSP 21489) is used to control the system and perform on-board processing. Interface between the system and a personal computer is through a USB Hi-speed connection.

Section: RESEARCH PAPER

Keywords: Data acquisition; Digital Signal Processing; On-board processing

Citation: Pedro M. Pinto, José Gouveia, Pedro M. Ramos, Development, implementation and characterization of a DSP based data acquisition system with on-board processing, Acta IMEKO, vol. 4, no. 1, article 5, February 2015, identifier: IMEKO-ACTA-04 (2015)-01-05

Editor: Paolo Carbone, University of Perugia

Received December 9th, 2013; **In final form** April 13th, 2014; **Published** February 2015

Funding: Work supported by Fundação para a Ciência e Tecnologia, Portugal

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1. INTRODUCTION

The development of analog to digital converters (ADCs) was the cornerstone of a massive shift in the architectures of measuring systems and devices. In fact, the rapid development of fast ADCs capable of achieving resolutions above 10-12 bit has revolutionized the instrumentation and measurement field and can be considered as one of the crucial building blocks to our worldwide digital content driven society. The possibility to measure just about anything, sometimes with extremely reduced costs, has increased many times the deployment of sensor based measurement systems as well as the total amount of acquired data, the rapid development of signal processing algorithms to extract real-time information of the raw data, the use of data mining to analyze the results [1], sensor fusion to combine the measurements from multiple sources [2].

A data acquisition system is typically a system or device that can digitize an input electrical quantity at a given sampling rate. It can have multiple input channels with multiple or single input ranges. By far, most commercial systems are designed to acquire voltages. For multi-channel devices, the cheaper solution is to have a single ADC and sequentially connect (using a multiplexer) the input signals to the ADC input, thus enabling the acquisition of multiple channels with only one ADC. This solution, well suited for many applications [3] and frequently implemented even within multipurpose micro-controllers, reduces cost but is incapable of simultaneous acquisition and the inter-channel interference (cross-talk) is usually non-neglectable. The main alternative is to have a independent ADC for each channel and thus a unique signal path to the ADC for each input channel. This solution is more expensive but can have lower cross-talk and can perform simultaneous acquisition.

Commercial of the shelf (COTS) data acquisition devices are used together with a computer or in some sort of specialized integrated system such as VXI [4], PXI [5], VME [6], AXIE [7] or CompactRIO [8]. The main advantage of systems that are not computer based is that stricter timing issues and higher throughput can be achieved in those architectures which were specifically developed to deal with the specificity of measurements systems. Computer based systems are either PCI or USB based. While the former are used in desktop computers, the latter are more flexible and can also be used in portable computers. However, the throughput when using USB connections can limit the range of the combined set of number of acquired samples, sampling rate and ADC number of bits. LAN based devices (of which LXI [9] is a particular case) are more frequently available but their usage as not reached the initially predicted dissemination.

Data acquisition systems are currently the most important blocks in just about every measurement system. For example, they are used in power quality monitoring [10, 11], in impedance measurement and spectroscopy devices [12], in the characterization of energy-harvesting devices [13], in environment monitoring [14], in real-time reflectometry diagnostic [15], in fusion experiments [16], in power metering [17] and many other applications.

Most COTS data acquisition devices include some sort of micro-controller or processing unit that manages the communication with the ADCs, controls the input range and communicates with the system main processor (e.g., the computer). For applications where the signal processing is done in the computer, this local processor acts mainly as a gateway with little or no processing tasks executed in the actual system device (see for example, [18]).

However, in some applications, processing in the acquisition system is required. The reason behind this requirement is for example in large measurement systems with multiple channels, some data reduction must be made before the data can be managed and processed in a timely manner. For example, in power quality monitoring or power quality QoS (quality of service), the measurement nodes must acquire the samples continuously without interruption. This constitutes a challenge since sending the raw data to a computer or central processing unit, for processing is hardly possible when the grid can have hundreds of such devices spread out in a large area. Collecting all the data in one or more data centers and still achieve real-time processing is not feasible. In this situation, the best approach is to have each node with a processor capable of performing digital signal processing to detect events (in power quality monitoring) and store/transmit only the data of such events. In power quality QoS, the nodes should quantify the QoS in terms defined by the local power regulator and transmit only the final aggregate parameters at a given periodic interval. Another system example that requires processing near the acquisition level are the detectors in the Large Hadron Collider (LHC). The ATLAS detector [19] has about 90 million channels which requires multiple customized trigger levels and processing algorithms to reduce the amount of data that it collects so as to discard non-relevant or non-events and focus centralized storing and processing on the most promising data.

The goal of this work is to develop, implement and characterize a 16-bit four-channel multi-range simultaneous data acquisition system with on-board signal processing capabilities. To achieve this goal, a digital signal processor is used to control the entire system and perform the on-board processing. The system has to be able to execute simultaneous acquisitions at a maximum rate of 600 kS/s and have an analog bandwidth of 1 MHz. Multiple independent voltage ranges must be available to allow accurate measurement of signals with different dynamic ranges. The input channels are acquired differentially with impedance at low frequencies of 1 MΩ (single-ended) and 2 MΩ (for differential acquisitions) and must withstand a considerable level of incorrect usage (i.e., incorrect direct connection to the power grid) without damaging the system circuitry and still ensure operability (this means that no fuses should be used).

2. SYSTEM ARCHITECTURE

Generically, a data acquisition system can be divided in three blocks. In the first block, the signal conditioning circuit adapts the input signal before digitalization. This includes attenuation or amplification to account for different input ranges. Another important function of the conditioning circuit is to protect the system against non-ideal conditions, like overload, incorrect usage or electrostatic discharge (ESD). In the second block, after the conditioning circuit, the analog to digital converter (ADC) digitalizes the signal. In the third block, to control the

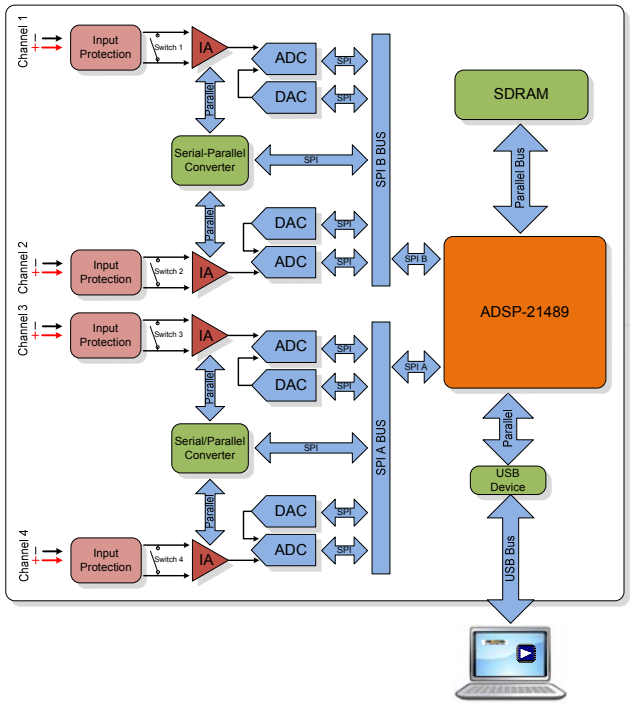

Figure 1. System architecture.

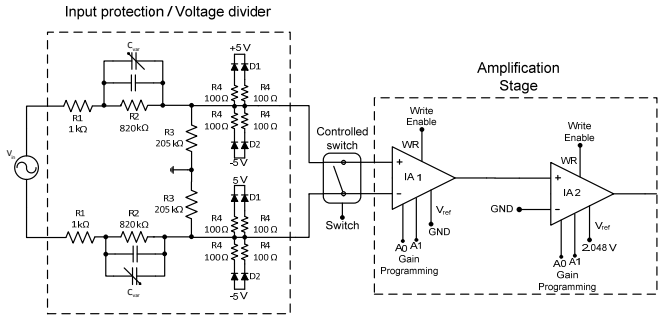

Figure 2. Analog signal conditioning circuit.

system a microcontroller is used. It can be a PIC - Peripheral Interface Controller [18], DSP - Digital Signal Processor [20], ARM [21] or FPGA - Field Programmable Gate Array [22, 23]. This device is responsible for the configuration of the range of each channel, by programming the amplifiers' gain, controlling the sampling frequency, collecting and transferring the sampled data. In some cases, the system has the ability to process data and control other systems, like actuators for example. In the system described in this paper, the control unit must be able to perform on-board processing such as FFT calculation for example and so, a DSP was selected.

In Figure 1, the proposed system architecture is shown. The system has four identical input analog channels, with independent gain setting and offset compensation, and individual ADCs. In addition to the described modules, the system has a 16 Mbit flash module to store the DSP program which is loaded upon reset or booting. A DSP external memory module (SDRAM with 256 Mb capacity in 16-bit words) was added to increase storage capacity and further increase flexibility in the processing of large amounts of data. USB 2.0 Hi-speed is used in the communication with an external computer. In the system, it is implemented using a FT2232H device. The speed of this interface limits the maximum sampling rate in continuous acquisition mode, when all the samples are to be transferred to the computer.

2.1. Analog interface circuitry

The input attenuation/protection circuit is shown in Figure 2. Its purpose is to attenuate the input signals 5 times and to protect the amplifiers, the ADCs and the DSP from incorrect usage [24]. It is dimensioned to sustain input direct connection into the power grid without any system damage and complete operability afterwards. This means that the user can incorrectly connect the system inputs into

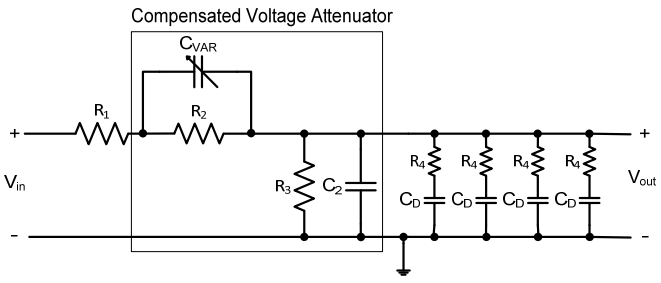

Figure 3. Equivalent analog input circuitry for single-ended acquisitions.

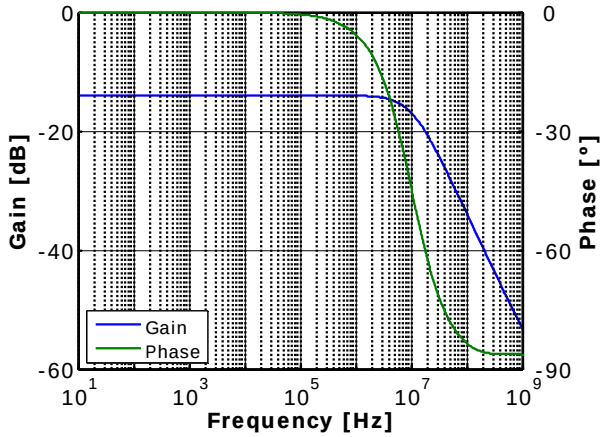

Figure 4. Simulation results of the gain of the analog input circuit before the ADC.

the power grid without damaging the device. Note that, the system will only operate correctly with input voltages up to ±10 V. The purpose of the input attenuation/protection circuit is so that the system is not damaged if it is incorrectly used (up to the power grid voltage). Therefore, the maximum operating range is ±10 V and the absolute maximum rating input voltage is ±325 V ($230\sqrt{2}$ V). The set R_2, R_3, C_{var} and the equivalent input capacitance from R_3 onward, form the basis of a compensated attenuator as is traditional for instance in the analog input attenuation of oscilloscopes. The schottky diodes (D_1) are included to protect over voltages from reaching the programmable amplifiers. R_1 and R_4 are included to ensure that during transient connection, and while the capacitors are discharged, the maximum current in the protection diodes do not cause their failure.

Although the inclusion of R_1 (as shown in the equivalent circuit for single-ended acquisitions represented in Figure 3 where C_D are the equivalent capacitance of the diodes and C_2 is the combined input capacitance of IA1 and of the offset compensation controlled switch) makes the voltage divider uncompensated, its value is dimensioned so that the extra poles (located at 10 MHz and 887 MHz) and extra zero (located at 796 MHz) are at frequencies well above the specified target input analog bandwidth (1 MHz). Note that the value of R_1 is selected as a compromise between the location of the lowest pole (at 10 MHz) and the current limit of the diodes.

With this set of parameters, the amplitude response of the input attenuator (including R_1 and the influence of the diodes) remains essentially constant until at least 1 MHz. The frequency response of the circuit was simulated and the amplitude and phase response are shown in Figure 4. The DC gain of -14 dB corresponds to the 1/5 gain desired for the input attenuator and the first pole is located at 10 MHz. The phase does not reach -90° because, at 100 MHz, the influence of the other pole and the zero is already changing the initial 1st order low pass filter like response.

As shown in Figure 2, two instrumentation amplifiers (IA) are used in each channel. Each of the IA are AD8250

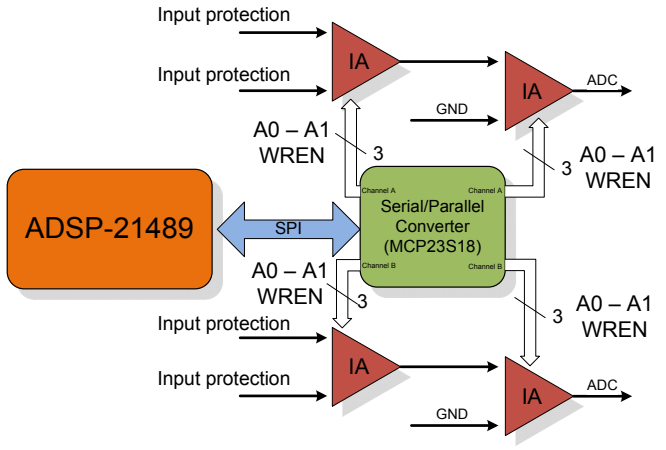

Figure 5. Detail of gain programming stage.

with programmable gains of 1, 2, 5 and 10, slew-rate of 20 V/μs and CMRR of 80 dB. The gain combinations from the two amplifiers enable the implementation of the nine input ranges listed in Table 1. Note that, for all ranges, the input signal is always attenuated five times by the input resistive divisor (see Figure 2). For example a $\pm$1 V input sine signal becomes a $\pm$0.2 V sine signal after the fixed gain attenuator and, in the $\pm$1 V input range, is amplified 10 times (fourth column of Table 1) to become a $\pm$2 V sine signal. Note that, in the last IA a 2.048 V DC component is added before the ADC converts the signal into the digital domain. Although it is counterproductive to attenuate a signal and then amplify it, this solution ensures the level of protection against misuse of the device that the system is capable of withstanding.

Each IA gain is set by the DSP using a SPI connection and a serial/parallel converter (one for each channel pair) as shown in Figure 5 and as it is directly related with the input range desired by the user. The IA gains are set before acquisition starts which means that this process is not time critical as the range is not changed during an acquisition. Therefore, the use of a slow serial to parallel converter is well suited as it also reduces the usage of I/O ports of the DSP. Three bits are used for each IA (two for the gain bits and one for the write enable).

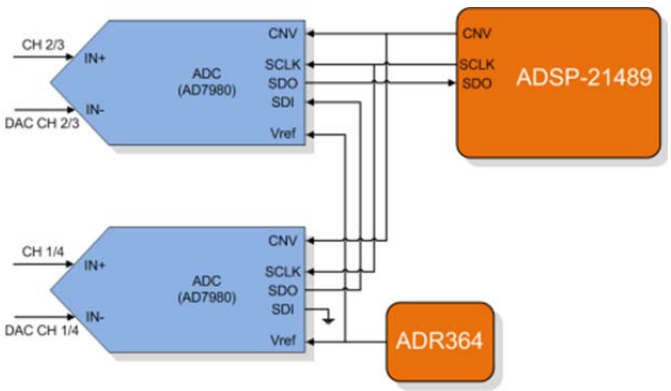

Figure 6. ADC daisy-chain connection. Each pair of ADCs shares the same SPI connection to the DSP.

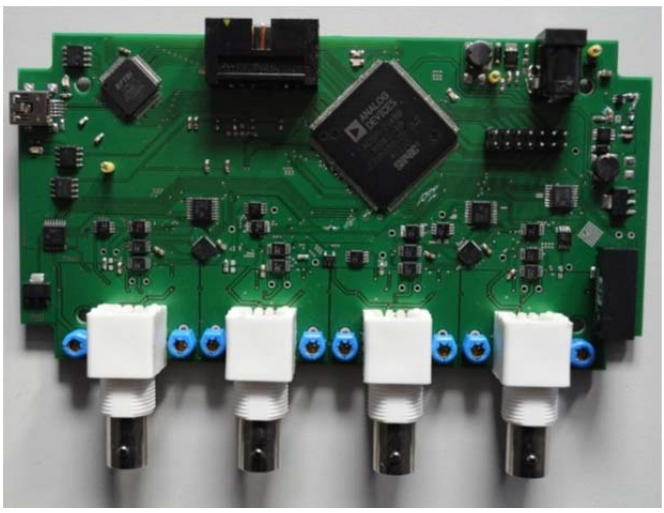

Figure 7. Implemented system. The final PCB has 145 mm length and 75 mm width.

2.2. Conversion into the digital domain

The selected ADCs (Analog Devices AD7980) are 16-bit SAR with maximum sampling rate of 1 MS/s, unipolar input voltage, -3 dB input bandwidth of 10 MHz, SPI interface with the ability of operation in daisy-chain configuration (as shown in Figure 6) to share a SPI connection. Note that, due to the method of operation of the selected SAR ADCs, no sample and hold is required. The ADC range is set to [0 ; 4.096] V and as mentioned, the V_{ref} input of the final IA (see Figure 2) is used to add the DC component (2.048 V) necessary to ensure a unipolar signal at the ADC inputs. In the digital domain, this fixed value DC component is removed, and the gain introduced in the analog amplification stage is removed from the ADC output as each 16-bit sample is converted into the voltage at the channel input taking also into account the gain introduced by the IAs.

2.3. Final prototype implementation

The final prototype implemented in a printed circuit board (PCB) is shown in Figure 7. In the bottom part of the picture, the four BNC connectors for each channel are visible. In the top middle section of the PCB is the DSP

Table 1. List of input ranges and corresponding gains of the instrumentation amplifiers and total analog gain (including also the input attenuator).

Input Range	IA 1 gain	IA 2 gain	IA Total Gain	Total Gain
±0.1 V	10	10	100	20
±0.2 V	10	5	50	10
±0.4 V	5	5	25	5
±0.5 V	10	2	20	4
±1 V	5	2	10	2
±2 V	5	1	5	1
±2.5 V	2	2	4	0.8
±5 V	2	1	2	0.4
±10 V	1	1	1	0.2

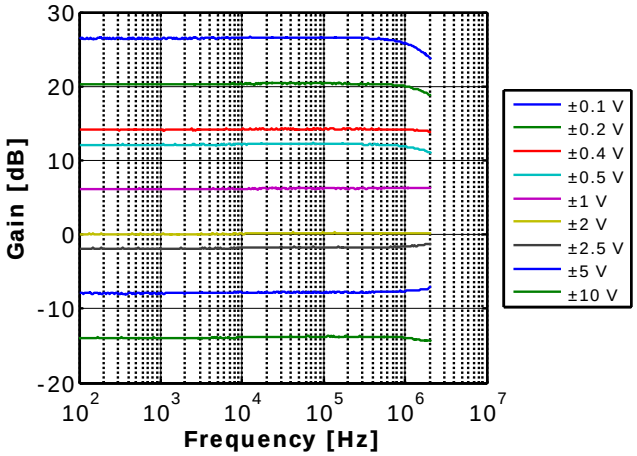

Figure 8. Input frequency responses for all ranges in one channel. The results for the other channels are identical.

while in the left-hand side is the USB communication integrated circuit (the USB connector is just to the left of the IC in the board edge).

The system JTAG connector is located in the top center of the PCB. Note that, once the system 16 Mbit flash module is programmed, the JTAG is no longer needed since, upon restart, the DSP program is loaded from the flash and executed. The JTAG is used for loading new programs, for testing and for programming the flash once the final firmware is ready.

3. SYSTEM CHARACTERIZATION

The frequency response of the acquisition channel (including the analog circuitry and the ADC) was measured with a TTi TG1010A function generator controlled with IEEE 488.2 and an application specifically developed in LabVIEW to control the function generator, set the channel input range, retrieve the DAQ samples and process the results. The processing stage includes the estimation of the measured signal amplitude using a simple, single-channel sine-fitting algorithm [25]. This characterization application then changes the stimulus frequency and automatically repeats the process for all measurement

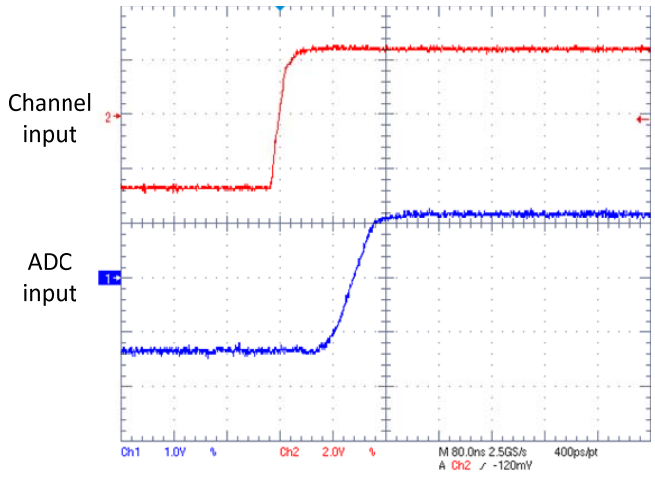

Figure 9. Delay/rising time measurement.

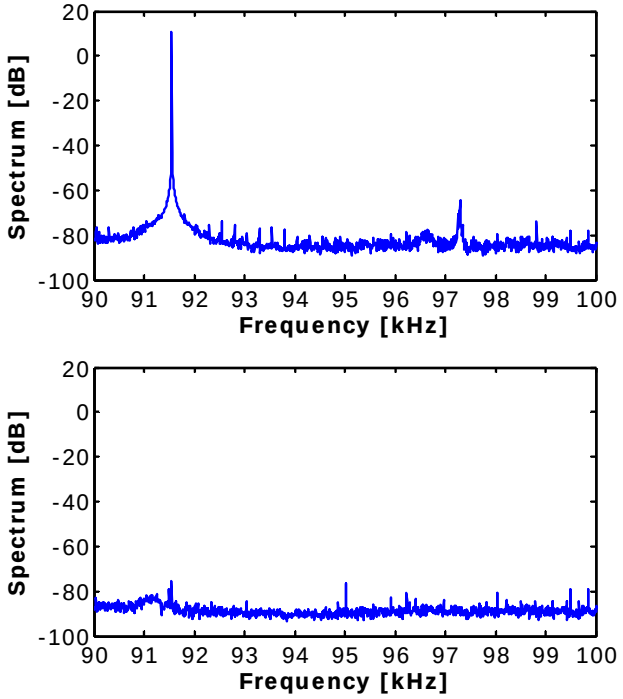

Figure 10. Measured average spectrum cross-talk measurements for 91.5523 kHz. The top average spectrum represents the input sinusoidal signal while the bottom average spectrum is the one obtained on the non-stimulated channel.

frequencies (selectable in the LabVIEW front panel) and all DAQ input ranges (also changing the signal generator output amplitude to match 95% of the dynamic input range for each DAQ range). The final results for one of the input channels and for all the input ranges are shown in Figure 8.

It can be seen that the overall input channel bandwidth is limited by the response of the lowest range and corresponds to about 2 MHz. However, a slight distortion was measured for signals with frequencies above 1.6 MHz due to the slew-rate of the amplifiers. Nevertheless, these limits ensure that the specified 1 MHz input signal bandwidth, for all ranges, is achieved. The results for the remaining three channels are similar.

The delay/rising time response of one of the channels (before the ADC) was measured with a TTi TG1010A function generator and a 350 MHz TDS5034 oscilloscope. The results are depicted in Figure 9. The rise time is 57.4 ns while the delay is 112 ns. As will be shown in the simultaneous acquisition measurement, these values are within the order of magnitude of the interchannel delay and therefore are considered acceptable. Note that the main cause of the rise time and delay are the capacitors used in the analog input compensated attenuator C_{var} and of the equivalent capacitance C_2.

To characterize the inter-channel cross-talk, a sine signal near the full-input range of the DAQ is applied to one channel while the others are short-circuited. The ratio between the generated sine amplitude and the amplitude measured at that same frequency in the other channels is a quantification of the inter-channel cross-talk. To improve the estimation of the cross-talk value, multiple acquisitions are performed and the average spectrums are used. In Figure

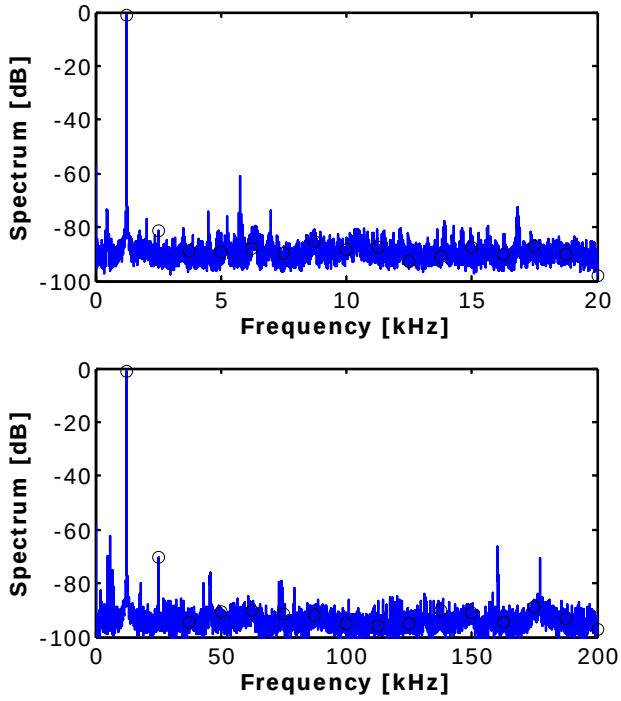

Figure 11. Measured average spectrum THD measurements. The circles represent the detected harmonic amplitudes. The top spectrum corresponds to a 1250 Hz sine signal acquired at 40 kS/s and the resulting THD is -79 dB. The bottom spectrum corresponds to a 12.5 kHz sine signal acquired at 400 kS/s and the resulting THD is -72.1 dB.

10, the results from one of the cross-talk measurements are presented. The stimulus signal is a 91.5523 kHz sinusoidal signal. In this case, the cross-talk is -86.3 dB. Typical cross-talks of around -80 dB were achieved for all tested situations.

The frequency value was selected to minimize spectral leakage (500 kS/s with 65536 samples correspond to a frequency resolution of 7.63 Hz and with this frequency, the fundamental will appear in the FFT at the 12000 bin). Also the frequency was selected to be representative of the input frequency range and to avoid any overlap (caused by aliasing) from any input signal higher harmonics. Note that, multiple tests at different frequencies were also performed and it is from these tests that the overall -80 dB crosstalk value was obtained.

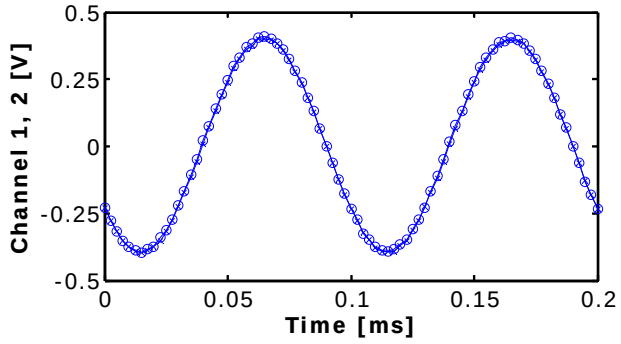

Figure 12. Simultaneous acquisition of a 10 kHz signal. Both channels are represented (the channel 1 samples are the circles and the samples from channel 2 are the crosses).

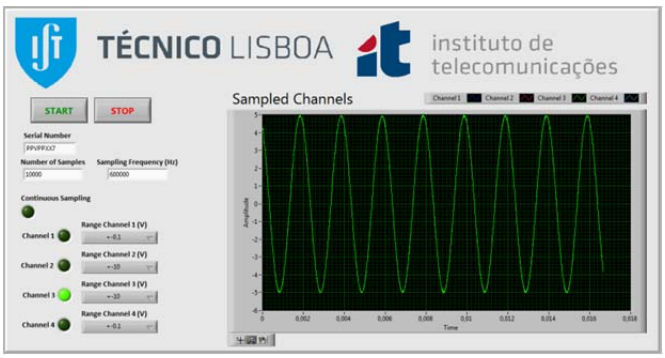

Figure 13. Front panel of one acquisition example.

In addition to the cross-talk evaluation, a study in the harmonic distortion introduced by the system was also performed. This characterization was done with a low-distortion function generator from Stanford Research Systems (a DS360) with THD better than -100 dB (until 20 kHz). The results from two situations are shown in Figure 11. The first situation corresponds to a 1250 Hz sine signal with 1 V amplitude and acquired at 40 kS/s. The measured THD (using 10 records to average the amplitude spectrum) is -79 dB. In the second situation, the frequency is changed to 12.5 kHz (the sampling rate is also increased 10 fold) and the resulting THD is -72.1 dB.

4. MEASUREMENT RESULTS

To demonstrate the simultaneous acquisition of the developed DAQ, a 10 kHz sinusoidal signal was applied to all channels as they were acquired with a sampling rate of 400 kS/s. In Figure 12, two of the channels are depicted. In this case, the interchannel delay estimated using the seven-parameter sine-fitting algorithm [26], is under 125 ns.

In Figure 13 one example of an acquisition, as shown in the front panel of the developed LabVIEW interface application, is shown. The application enables the selection of the channels to be acquired, their independent ranges, the number of samples and the sampling rate.

In Figure 14, the amplitude of the FFT calculated within the device is shown. The input signal corresponds to a sinusoidal or triangular signal with 1 kHz and amplitude of 0.4 V (generated by a Agilent 33210A) sampled at 40 kS/s with 65536 samples.

5. CONCLUSIONS

The development, implementation and characterization of a simultaneous data acquisition system with four-channels, multiple independent ranges, analog bandwidth of at least 1 MHz, sampling rate up to 600 kS/s and advanced on-board processing capabilities is presented. Multiple results demonstrating the developed system characterization and performance were presented. The device can be used as a development tool for advanced measurement systems requiring embedded processing such as PQ monitoring and PQ QoS measurements.

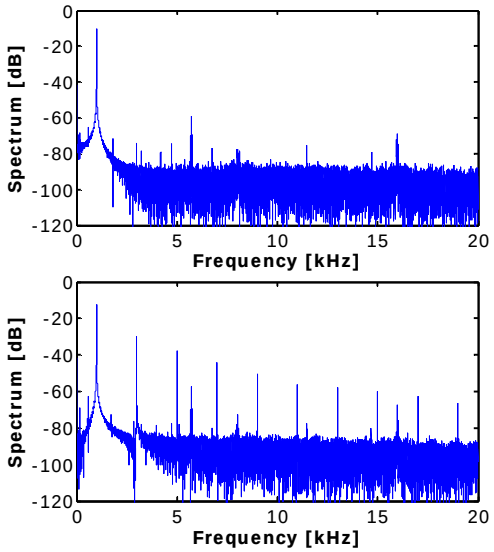

Figure 14. Example of FFT calculation done within the data acquisition device. Sinusoidal signal (top) and triangular signal (bottom).

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