

Architecture of the multi-tap-delay-line time-interval measurement module implemented in FPGA device

Marek Zieliński, Maciej Gurski, Dariusz Chaberski

Institute of Physics, Faculty of Physics, Astronomy and Informatics, Nicolaus Copernicus University, Grudziadzka 5, 87-100 Torun, Poland

ABSTRACT

This paper describes the architecture of a Multi-Tap-Delay-Line (MTDL) time-interval measurement module of high resolution implemented in a single FPGA device. The new architecture of the measurement module enables to collect sixteen time-stamps during a single measuring cycle. It means that the measured time-interval can be precisely interpolated from the collection of the sixteen time-stamps after each measuring cycle. Such architecture of the measurement module leads directly to an increased resolution, to a limited total measurement time and a decreased duty cycle of the measurement instrument.

Section: RESEARCH PAPER

Keywords: time-interval measurement, tapped delay lines

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Corresponding author: M. Gurski, e-mail: gural@fizyka.umk.pl

1. INTRODUCTION

High resolution Time-Interval Measurement Systems (TIMS) are widely applied in many system. For example they can be applied in quantum cryptography experiments, in the characterization of clock phase fluctuations, in life-time measurements of the excited atomic states, in ultrasonic flow-meters or monitoring systems of time-of-flight mass spectrometers [1-8]. Limiting the total number of time-interval measurements and increasing at the same time the system resolution, the effective duty cycle and the total power consumption could be decreased [9].

The system saves energy in two ways. Firstly, measurements are realised in parallel, so the measuring time is shorter and the energy consumption is lower. The second way of energy consumption depends on a selective module turning-on. This procedure is especially profitable because every module that can be turned-off (no power delivered) or can go into stand-by mode (no standard clock provided) when it is not used elongates the working-time with the same battery set. Some areas of a Field Programmable Gate Array (FPGA) device can be turned off. The system is

designed in such a way that the system parts that are used selectively in time are implemented into those FPGA areas that can be turned off without any influence on the whole system operation.

For example the calibration module can be removed (turned off) after calibration is done, so the power consumption can be decreased, which extends battery life-time.

The measurement memory must be turned on as long as the measurement series has not been read by the computer even when no write process is realised.

Without these procedures the FPGA consumes 4.4 W of power and with the procedures described above the energy consumption lowers to 0.65 W.

The measurement system presented in this paper enables not only an increasing system resolution but also a significantly decreasing uncertainty of the single time-interval measurement.

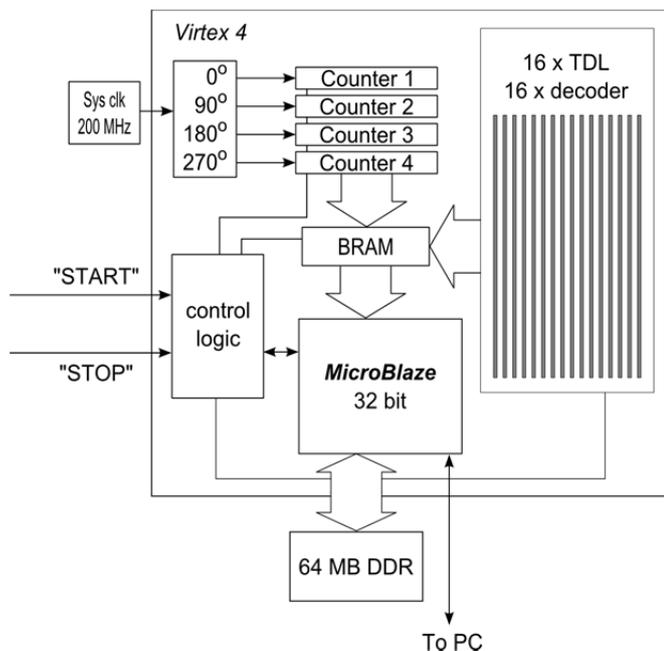


Figure 1. The block diagram of TIMS.

2. ARCHITECTURE OF THE TIMS

TIMS as a virtual instrument consists of a hardware unit, flexible software and a computer. The block diagram of the new TIMS architecture is shown in Figure 1. The system is implemented using the Xilinx Virtex 4 FPGA structure and uses chip-outside-located 64 MB DDR of RAM for data collection.

The main unit of the system is a 32 bit soft processor – MicroBlaze. Other parts of the system are implemented as microprocessor peripherals. ISE and EDK programming tools have been used for the implementation of the virtual microprocessor (MicroBlaze), that has been programmed in

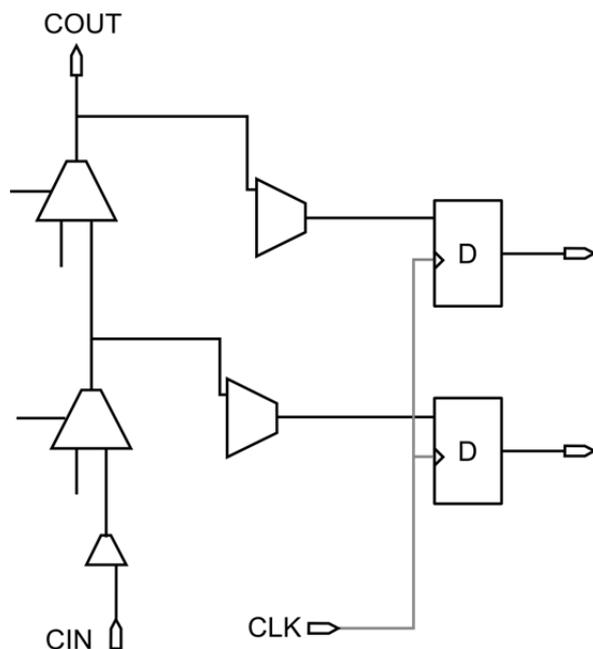


Figure 2. Two taps of TDL made of carry-chain with registers before tuning.

C language and its peripherals.

The implemented system consists of a group of sixteen two-hundred-element multi-tap delay lines with coupled registers, sixteen code converters, four clock cycles counters, blocks of inside memory (BRAM), an interface and a control unit. A carry chain of CLBs (Configurable Logical Block) is used to tapped delay lines and register implementation (Figure 2). It is possible to change the placement of the elements and connections to change the line delay. Using this method, the characteristics of the delay-line can be shaped.

Data transferred to the personal computer is worked out by the Python-script-language that allows, in a simple way, to obtain a very efficient, multiprocessor programming environment. These scripts also generate corrected VHDL (Very High Speed Integrated Circuits Hardware Description Language) and UCF (User's Constraints File) source files, so the process of designing the measuring module is fully automated. Mainly the location of TDLs and the order of their output is corrected. The system can be calibrated without the need of reprogramming. The calibration module can be removed (turned off) after calibration is completed, so the power consumption can be decreased, which extends battery life-time.

First the taps must be sorted, because the time-of-clock (clk) net is not monotonic (Figure 3). The values read from the FPGA editor do not contain information about the fluctuations of the delays in the FPGA structure. For this reason, the system can read all TDL registers in raw mode, bypassing the code converter and storing them in BRAM. It is not possible to read all the sixteen TDL states at the same time (there are not enough BRAMs for this operation implementation on the chip that was used). There is a 16-to-1 multiplexer to switch between TDL's registers. Another signal multiplexer can connect either to the divided by N system clock (100 MHz) or an external pulse signal. The raw waveform of the recorded system clock is triggered by the divided by N built-in clock and then stored in BRAM. Data from BRAM are sent to the computer.

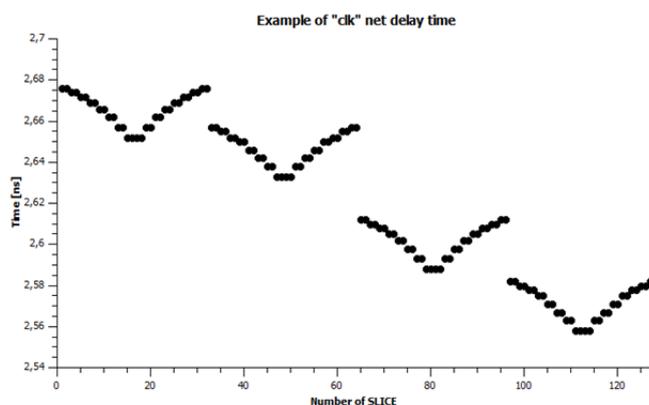


Figure 3. Example of "clk" net delay in FPGA device for 128 slices – read from the FPGA editor.

The calibration program on the PC computer is seeking anomalies (bubbles) in the waveform (Table 1). The anomalies can be single, double and so on. Reordered zeros or ones usually appear at the beginning and at the end of every sequences obtained for the same values. The program uses a special correlation procedure to obtain the right order of all taps implemented in the FPGA structure. The next procedure generates VHDL code of the sorted TDL. This procedure is repeated for every TDL. After compilation the corrected TDLs are implemented in the FPGA.

Quadrupling of the clock cycle counter ensures a sufficient set-up time during incrementation and the possibility of asynchronous read-out of data from one of the counters. The most proper counter is being chosen on the basis of the information obtained from a particular TDL. These data are used for computing all sixteen time-stamps from all TDLs.

Each measured time stamp consists of a main part, which is taken from one of the clock cycle counters, and a residual part, which is taken from one of the TDL-registers and then compressed to binary-natural-code. The theoretical precision of the TDL is 25 ps.

There is a great need to implement the code converter, which converts from thermometric to binary-natural-code. The main reason to use the code converter is limitation of the data memory size and speed of data transfer. Single time-interval measurements can generate more than four hundred bytes of data. This value is similar in size to the capacity of the single BRAM on the chip. The code converter reduces about hundred-fold data for storage.

Requirements for a code converter are to reach a compromise between speed and space occupancy on the FPGA chip. To achieve this in any converter 16-to-4 bits conversions in parallel mode were implemented. Finally, the chosen code-converter requires only two BRAMs for one TDL in comparison to more than six without code converter.

The DDR SDRAM 64 MB of capacity is used for data acquisition. In case when there are more than five hundred time stamps in one series and the intensity of measurement of time-intervals is too fast (more that 100 k samples per second) data are sent to the PC indirectly through the DDR SDRAM, which allows obtaining about four thousand times more space for measurements.

3. PRINCIPLE OF TIME-INTERVAL MEASUREMENT

The main task of the measuring system is registration and collection of time-stamps. The time-stamp is combined from two parts.

The first one expresses the total number of standard-clock periods that have appeared from measuring module initialization - it can be called standard-clock period counter. This measuring stage is realized by four mutually-complementing counters-register pair. The second part, that is realized with the use of tapped-delay-lines, expresses the standard-clock phase when the event occurred. The value of the second part is proportional to the index of the bit

Table 1. The exemplary section of waveform before sorting a) and after sorting b) the taps 97, 98 and 100 are accordingly shifted into place and now their taps numbers are respectively 100, 97, 98.

a)

No.	Numer of tap											
	93	94	95	96	97	98	99	100	101	102	103	104
0	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	0	1	0	0	0	1	1	1	1
2	0	0	0	0	1	0	0	0	1	1	1	1
3	0	0	0	0	1	0	1	0	1	1	1	1
4	0	0	0	0	1	0	1	0	1	1	1	1
5	0	0	0	0	1	0	1	0	1	1	1	1
6	0	0	0	0	1	0	1	0	1	1	1	1
7	0	0	0	0	1	0	1	1	1	1	1	1
8	0	0	0	0	1	0	1	1	1	1	1	1
9	0	0	0	0	1	0	1	1	1	1	1	1
10	0	0	0	0	1	1	1	1	1	1	1	1

b)

No.	Numer of tap											
	93	94	95	96	98	100	99	97	101	102	103	104
0	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	1	1	1	1	1
2	0	0	0	0	0	0	0	1	1	1	1	1
3	0	0	0	0	0	0	1	1	1	1	1	1
4	0	0	0	0	0	0	1	1	1	1	1	1
5	0	0	0	0	0	0	1	1	1	1	1	1
6	0	0	0	0	0	0	1	1	1	1	1	1
7	0	0	0	0	0	1	1	1	1	1	1	1
8	0	0	0	0	0	1	1	1	1	1	1	1
9	0	0	0	0	0	1	1	1	1	1	1	1
10	0	0	0	0	1	1	1	1	1	1	1	1

which is set and is followed by bits that are cleared. The measured time-interval Δt_m is calculated by the difference of two time-stamps.

The precision of TIMS in practice depends on the precision of interpolators, that measure residual time intervals and accumulated jitter of the standard clock [9]. If multi-tap delay lines are used in the design of the interpolator then the value of the single segment delay τ and its standard deviation determines the precision of the time-interval (Δt_m) measurement. If the interpolator consists of n delay lines of relatively high resolution, then during a single measuring cycle it is possible to obtain n different results of time-intervals Δt_m [10, 11]. Such solution leads directly to an increase of precision of the time-interval

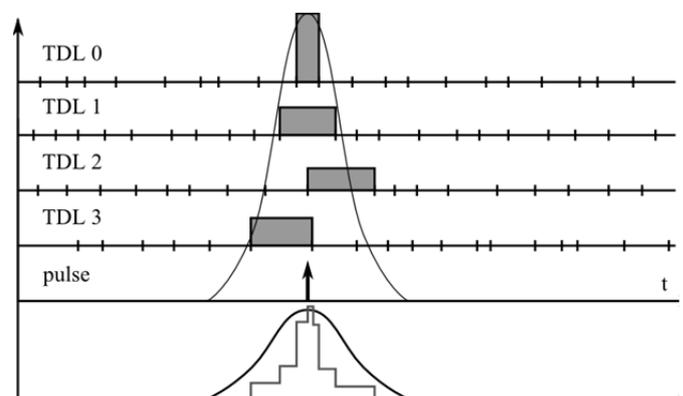


Figure 4. The idea of multiple TDLs measurement.

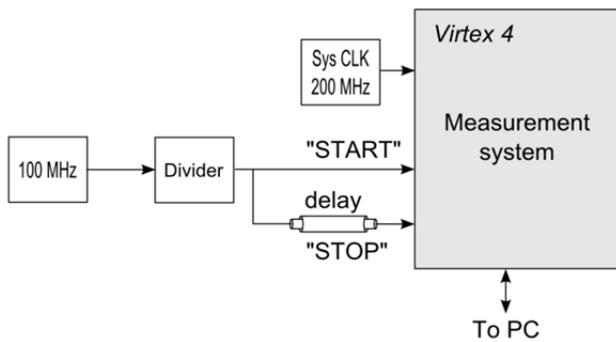


Figure 5. The experimental measurement system.

measurement and reduces the number of measurement cycles. This method significantly reduces the power consumption for battery-powered systems, because the number of measuring cycles is generally significantly decreased. Knowing delay line characteristics such as DNL (Differential Nonlinearity) and INL (Integral Nonlinearity) and using the quantization-and-nonlinearity-minimization (QNM) method, it is possible to obtain a two-sample-difference histogram, increased system resolution and decreased uncertainty of the time-interval measurement [12].

In the presented system with 16 TDLs which consists of 200 taps (for each TDL), the expected accuracy should be better than 15 ps for a single-shot measurement.

4. EXPERIMENTAL RESULTS

A series of time-interval measurements was performed to verify the measurement system. For the test, a single section of coaxial cable was used as a delay element as is shown in Figure 5.

Figures 6 and 7 show time-stamp histograms obtained for start and stop pulses. One should notice that the surfaces of both diagrams are equal to the number of TDLs. Figure 8 shows the time-interval histogram obtained as a difference between start and stop measurements. It is worth being noticed that the uncertainty of the time-interval does

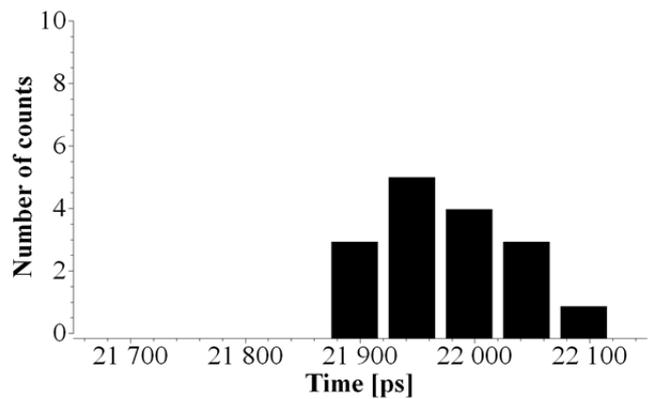


Figure 7. Time-stamp histogram obtained for stop pulse.

not increase significantly in comparison to the source time-stamp uncertainties.

5. CONCLUSIONS

Designed time-interval measuring system allowed to obtain a higher precision of measurements thanks to simultaneous measurements by 16 TDLs at the same time. Measurements for every hit are realized in parallel, so the measuring time is not increased, and the energy consumption is reduced because the measuring module can go periodically in stand-by mode for a longer time.

The obtained time-interval histograms are characterized by a low uncertainty in comparison to time-stamps uncertainties even though TDLs characteristics are very nonlinear, because the QNM method takes into account the characteristics of the TDLs.

The design process of the measuring module has been fully automated, which is especially useful for TDLs implementation. The TDL output wires are automatically rotated to obtain proper thermometric codes that allows the implementation of TDLs with a precision equal to one carry element delay.

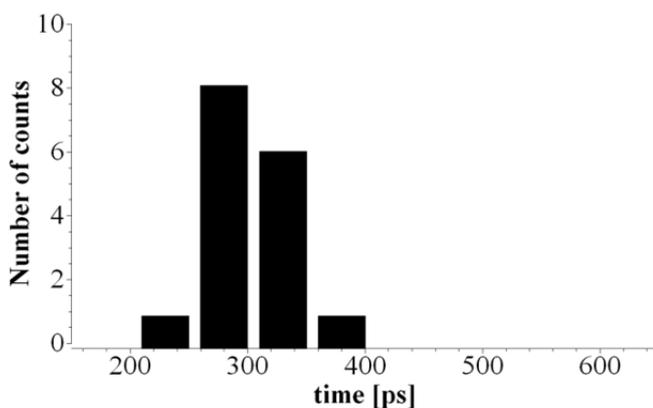


Figure 6. Time-stamp histogram obtained for start pulse.

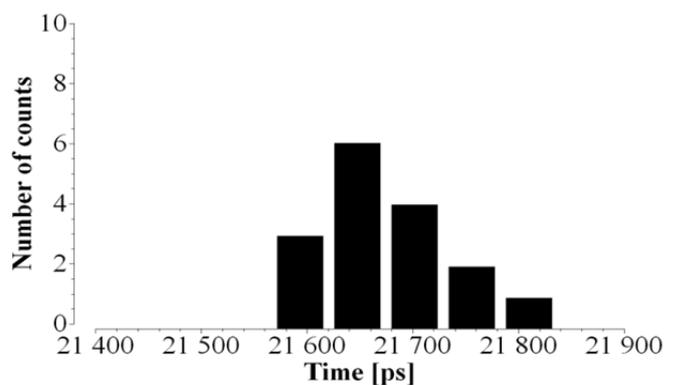


Figure 8. Time-interval histogram.

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