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Time coordination of standalone measurement instruments by synchronized triggering

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ABSTRACT
A Hardware Interface (HI) to synchronize the operations of standalone Measurement Instruments (MIs) in the absence of networking has been proposed in the recent literature. The synchronization accuracy achieved is one period of the clock equipping the HI. To improve the synchronization accuracy two solutions can be argued on the basis of the mathematical model of the delay between HIs. The first involves increasing the clock frequency; the second concerns the compensation of the phase delay between HI clocks. In this paper the second solution is adopted in order to: (i) reduce the energy consumption, and (ii) not increase the complexity of the hardware architecture. The phase delay compensation is obtained by introducing a programmable delay line after the HI clocks. The phase delay evaluation and the successive tuning of the delay line are performed in the synchronization phase of the HIs. Once synchronized, each HI is moved to the standalone MI to trigger it according to the common sense of time. During the execution of the measurement procedure, networking is not necessary. Experimental tests validate the correct operation of the upgraded HI architecture and indicate that the achievable synchronization accuracy is a low percentage of the HI clock period.

Section: RESEARCH PAPER

Keywords: Synchronization; Embedded hardware; Standalone Measurement Instrument; Distributed Measurement System

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1. INTRODUCTION

In [1] the Hardware Interface (HI) architecture was proposed to bring the common sense of the time to the standalone Measurement Instruments (MIs) [2], [3] in operative scenarios in which no stable network is available. The time coordination of the operations of MIs is difficult when: (i) the network topology does not provide a continuous, reliable and stable link, wired or wireless, to the whole network [4]-[15], (ii) the installation of new wired or wireless links or repeaters would be expensive or not physically or technically possible [16]-[19], and (iii) a time constraint requires both fast and efficient solutions [20]-[22]. In these cases, no network services are available for the standalone MIs and synchronization services based on packet exchange as the std. IEEE1588 cannot be used [23].

The HI architecture includes a counter driven by a clock, and a Programmable Interface Controller (PIC). The HIs are synchronized by enabling the HI counters at the same time. After that, the HIs are moved and connected to the standalone MIs that can be in different places where no networking is available. The time coordination of the measurement operations is achieved by triggering the MIs in synchronized modality.

The software and hardware architecture of the HI are designed so that (i) the random effects of the operating system are avoided, and (ii) the polling cycle to check the trigger condition is reduced [24]-[26]. The result is that the synchronization accuracy between two triggers sent to the standalone MIs is one clock period.

In the paper, the mathematical model of the contribution of each hardware and software component to the synchronization delay is developed. The analysis of the mathematical model highlights that to improve the synchronization accuracy two

solutions can be argued: (i) increasing the clock frequency, and (ii) reducing the phase delay between clocks.

The first solution involves problems in the design of the HI [27], and increases the power consumption [28].

The second solution is more advantageous than the first and it is developed in this paper. To this purpose, the hardware architecture of the HI is upgraded by adding the programmable delay line after the clock block. This delay line permits realignment of the clock signals of the HIs once their phase delays are previously evaluated.

The phase delay evaluation and the successive tuning of the delay line are performed in the synchronization phase of the HIs. The first step of the synchronization phase concerns the evaluation and compensation of the clock delays by tuning the programmable delay line. The second step concerns the synchronized start of the counter block, as in [1]. During the synchronization, communication between the HIs is required. During the triggering of the MIs communication among HIs is not required and the synchronized measurement procedure can be performed also in the absence of networking.

The paper is organized as follows: in Section 2 the hardware architecture and the performed logical operations of the upgraded HI are presented; in Section 3 the mathematical model of the synchronization delay is analysed; in Section 4 the experimental results are discussed; finally, conclusions are drawn in Section 5.

2. OPERATIONS PERFORMED BY THE UPGRADED HI

The upgraded HI compensates the delay between the trigger signals sent to the MIs, as in [1], as well as the clock phase delays, to further reduce the synchronization delay.

The upgraded HI is composed by five blocks (Figure 1):

(i) Clock Block: drives the Programmable Interface Controller (PIC) and the Counter Block;
(ii) programmable delay line: compensates the phase delay between two HI clocks;
(iii) 8-bit Counter block: feeds the PIC with synchronized impulses;
(iv) PIC: generates the synchronized trigger signal on the pin RB1 for the MI. Moreover, it tunes the programmable delay line in the synchronization phase on the basis of the information sent by the Master PC;
(v) board Rabbit RCM4400W: operates as Wi-Fi interface between the HI and the Master PC. It is used only for the initial synchronization, and after that is disconnected from the HI.

The synchronization between two HIs is executed by the Starter block (Figure 1) and the Master PC on the basis of the procedure described in Subsection 2.1.

2.1. HI synchronization procedure

The synchronization procedure is organized in two successive steps.

The first step requires the connection among the Master PC, two HIs and the Starter Block, as shown in Figure 1.

The Master PC commands: (i) each HI to pull down the pin Tr_{OK} in order to inhibit the Start Count block, (ii) the Starter Block to measure the phase delay Δt_{ph} between the clocks of HI#1 and HI#2 connected to the pins Clk_1 and Clk_2 of the Phase Delay Measurement Block (PDMB).

The PDMB is equipped by an internal counter with period $T_{clk\_starter} = 5\ ns$ equal to 1/20 of the HI clock period that is

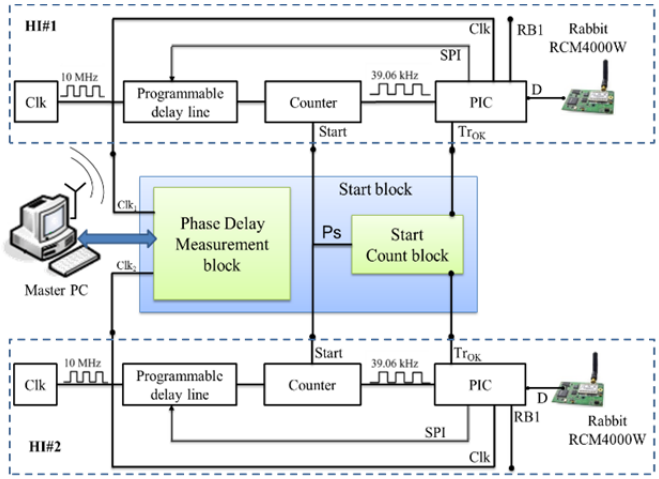

Figure 1. Block scheme of the connection among upgraded HIs, Starter Block, and Master PC in the synchronization phase.

100 ns. Therefore, the clock frequency of the starter block is 200 MHz. The mean value $\overline{\Delta t}_{ph}$ of 100 measures of the clock phase delay is sent to the Master PC by the Universal Serial Bus connection, and, successively, by the Wi-Fi interface to the HIs for tuning the programmable delay line.

Experimental tests indicate that after the synchronization, due to the hardware and software architecture of the HI and the starter block, the phase delay is lower than the resolution of the starter block (5 ns). In particular, by using a Digital Storage Oscilloscope with resolution 0.1 ns, the measured clock phase delay is 2.2 ns with standard deviation 0.9 ns. Increasing the number of measurements does not provide any advantage because the mean value does not significantly change and the standard deviation is less than the resolution of the starter block. The tuning procedure ends if:

$$\overline{\Delta t}_{ph} \le \max\left(T_{PDL}, T_{clk\_starter}\right) \tag{1}$$

where T_{PDL} is the resolution of the programmable delay line. This condition ensures that the tuning procedure ends in the case the measured phase delay cannot be further evaluated, if $\overline{\Delta t}_{ph} \le T_{clk\_starter}$, or compensated, if $\overline{\Delta t}_{ph} \le T_{PDL}$.

Once the phase delay is compensated, the second step of the synchronization procedure starts. As in [1], the Master PC sends the following trigger conditions to the two HIs:

- n_{iip} number of impulses that the PIC must count before triggering the MI,
- n_m number of repetitive measures to be executed by the MI,
- ν_m number of impulses between two consecutive measures.

In order to execute synchronized measurement operations it is necessary that n_{iip} and n_m are identical for both the HIs. Once this information is received, the HI pulls up the pin Tr_{OK}.

When both the pin Tr_{OK} of HI#1 and HI#2 are high, the pin Ps of the Start Count block is pulled up and the Counter block of each HI starts.

The signal on pin Ps is sent to the HIs in parallel connection, guaranteeing that the delay between the start of the Counter blocks is determined only by their hardware characteristics.

Once the PICs receive the impulse, the HIs can be disconnected from the Starter block and connected to the standalone MIs.

The Wi-Fi connection is involved in the synchronization process of the HI only for the transmission of the trigger generation parameters (n_{itp}, n_m, ν_m) and the measured phase delay for the tuning of the programmable delay line. Therefore, the Wi-Fi interface does not influence the synchronization accuracy. As a consequence, any boards implementing the conversion Wi-Fi-Serial communication can be used.

2.2. Triggering procedure

The time coordination among the operations executed by the MIs is obtained by the synchronized trigger signals sent by the HIs.

At the beginning, each HI set n_{itp} and after that generates the trigger signal. Successively, all the HIs start the count simultaneously. The program set up in the PIC counts the counter impulses and checks whether the actual count is equal to the set-up value. These operations are performed before the successive impulse occurs. This reduces the effect of the polling to check the trigger condition.

Figure 2 shows the block diagram of the operation performed by the PIC:

1) the internal variable i is incremented;
2) if $i = n_{itp}$, then HI sends the trigger signal by generating an impulse signal in the RB1 line, and the new values are updated $n_{itp} = n_{itp} + \nu_m$, $n_m = n_m - 1$;
3) else go to step 1;
4) if $n_m = 0$, the triggering procedure ends.

3. SYNCHRONIZATION DELAY ANALYSIS

The synchronization delay ΔT between two triggers is determined by the hardware architecture of the two HIs and the time needed to execute their operation (Figure 3). It is [1]:

$$\Delta T = \left(n_c T_{c1} + n_p T_{p1} + E_{P1}\right) + \\ -\left(n_c T_{c2} + n_p T_{p2} + E_{P2}\right) + O_C + O_P; \quad (2)$$

where:

- T_{c1} and T_{c2} are the clock periods of HI#1 and HI#2, respectively;
- T_{p1} and T_{p2} are the clock periods of PICs equipping HI#1 and HI#2, respectively;
- n_c is the counting number of HI#1 and HI#2, equal to $n_{itp}2^n$ where n is the number of bit of the counter;
- n_p is the number of elementary operations to execute the triggering procedure in the PIC;
- O_C is the start offset time between the counting on HI#1 and HI#2. It depends on Δt_{Ph} and the time instant t_1 and t_2 (Figure 4) corresponding to the opening of the counter

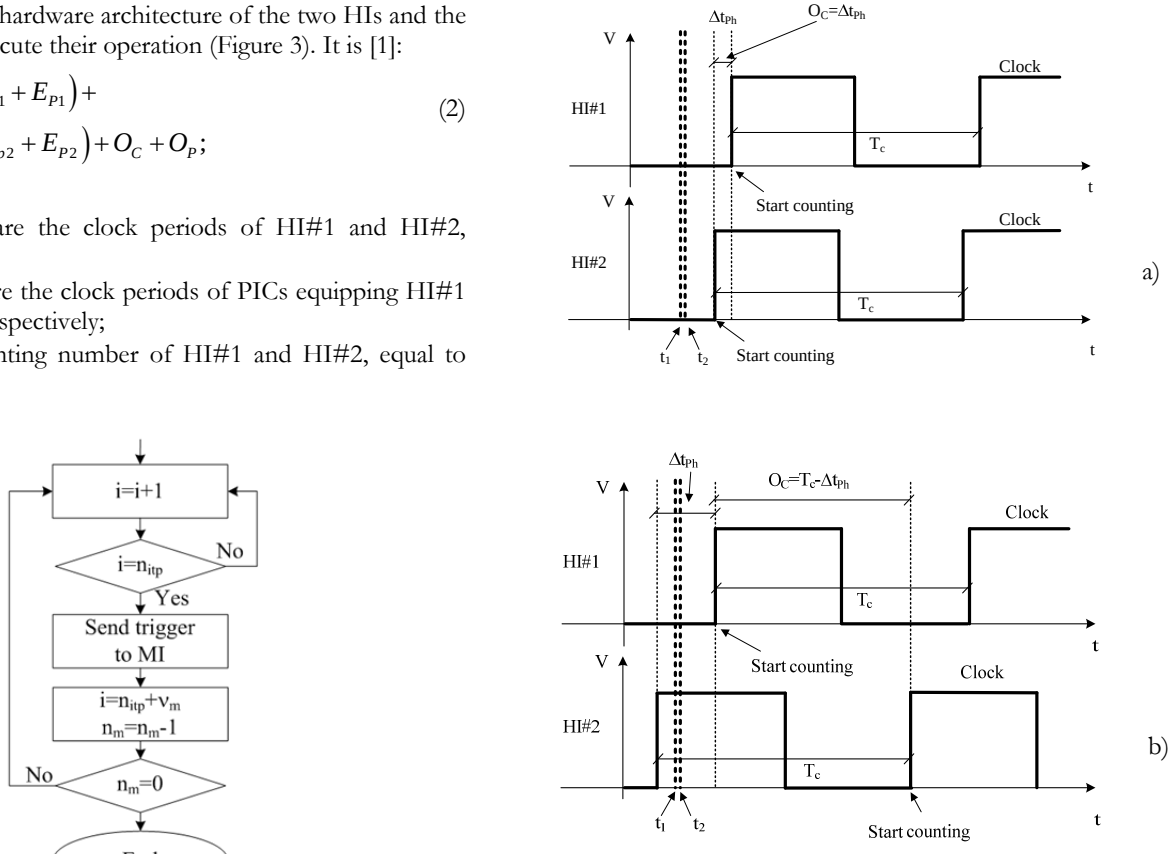

Figure 3. Unified modelling language diagram of the operations executed by the HI components involved in the synchronized triggering of the MIs.

Figure 4. Delay between the opening of the counter gate and the start of counting. a) t_1 and t_2 occur before the raising of the two clock signals, b) t_1 and t_2 occur between the raising of the two clock signals.

Figure 2. Block diagram of the performed operation by each HI for the synchronized generation of the trigger signal.

gate of HI#1 and HI#2, respectively;

- O_p is the start offset time between two PICs;
- E_{P1} and E_{P2} are the time intervals required by the hardware of the two PICs to pull up the pin RB1 and, then, trigger the MI.

Owing to the synchronized start of the counting, O_p has no influence in the evaluation of ΔT.

By considering the vector $\bar{x}$ made up of: n_c, n_p, T_{c1}, T_{c2}, T_{p1}, T_{p2}, E_{P1}, E_{P2}, O_C, the variation of the synchronization time delay (1) evaluated according to [29] is:

$$\Delta_{\Delta T} = \sqrt{\left(\left(n_c\right)\Big|_{\bar{x}} \Delta_{T_{c1}}\right)^2 + \left(\left(n_c\right)\Big|_{\bar{x}} \Delta_{T_{C2}}\right)^2 + \left(\left(n_p\right)\Big|_{\bar{x}} \Delta_{T_{p1}}\right)^2 + \left(\left(-n_p\right)\Big|_{\bar{x}} \Delta_{T_{P2}}\right)^2 + \Delta_{O_C}^2 + \Delta_{E_{P1}}^2 + \Delta_{E_{P2}}^2} \quad (3)$$

where:

- Δ_{Tc1} and Δ_{Tc2} are the variation range of the values of T_{c1} and T_{c2}, respectively,
- Δ_{Tp1} and Δ_{Tp2} are the variation range of the values of T_{p1} and T_{p2}, respectively,
- Δ_{EP1} and Δ_{EP2} are the variation range of the values of E_{P1} and E_{P2}, respectively.
- Δ_{Oc} is the variation range of the values of O_C.

Since the two HIs have the same hardware, it is:

$$T_{C1} = T_{C2} = T_C, \quad T_{P1} = T_{P2} = T_P$$
$$\Delta_{T_{C1}} = \Delta_{T_{C2}} = \Delta_{T_C}, \quad \Delta_{T_{P1}} = \Delta_{T_{P2}} = \Delta_{T_P} \quad (4)$$

Moreover, absence of conditional jumps and correlation between parameters can be assumed. In fact, to check the trigger condition in the software set up in the PIC there are no conditional jumps and the parameters in (2) are related to independent devices.

The variation range of Δ_{Tc} and Δ_{Tp} is according to the propagation delay of the hardware components and can be evaluated by their datasheet.

The variation range Δ_{Oc} depends on Δt_{Ph}. In particular two cases can occur:

- if t_1 and t_2 are before the raising edge of the clock signals (Figure 4a), $Oc = \Delta t_{Ph}$. Indeed, the counters of HI#1 and HI#2 are sensitive to the raising edges of the clocks that have lower delay;
- otherwise $Oc = Tc - \Delta t_{Ph}$ (Figure 4b). The gate of the HI#1 counter is opened before the occurrence of the raising edge of the HI#1 clock, the gate of HI#2 counter is opened after the occurrence of the raising edge of the HI#2 clock. Consequently, the HI#2 counter will be sensitive to the successive raising edge of the HI#2 clock.

Since Δt_{Ph} varies in the range [0, Tc], Δ_{Oc} varies in the range [0, Tc], also. Decreasing Δt_{Ph}, the probability that $Oc = \Delta t_{Ph}$ increases (Figure 4a). As a consequence, O_C value is decreased.

The programmable delay line permits the reduction of the variation range of Δt_{Ph} according to its resolution. As a consequence of the parallel connection among Starter Block and the two HIs, $|t_2 - t_1|$ is of some ps and then negligible with respect to Δt_{Ph}. In fact, $|t_2 - t_1|$ is determined by the propagation delay in the two cable lengths of (0.150±0.001) m connecting the pin Ps of the Starter Block with the start input pin of the HIs, and the difference between times to change the gate states. Owing to the propagation speed of the signal, the difference between t_1 and t_2 is about 5 ps. The difference between the times to change the gate states is in the order of 10 ps. Therefore, the difference between $t1$ and $t2$ is almost 15 ps, negligible with respect to Tc = 100 ns. It can be assumed that $t_1 \approx t_2 = t^*$. Due to periodicity of the clock signal the probability that t^* is included in the time interval T_C is 1. The corresponding probability density function is:

$$f(t) = \frac{1}{T_C}. \quad (5)$$

Consequently, the probability $\mathbf{p}$ that t^* occurs in the time interval Δt_{Ph} is [30]:

$$\mathbf{p} = P(0 < t^* < \Delta t_{Ph}) = \int_0^{\Delta t_{Ph}} f(t)\,dt = \frac{\Delta t_{Ph}}{T_C}. \quad (6)$$

By taking into consideration that at the end of the synchronization procedure Δt_{Ph}<5ns and Tc=100ns, it results in $\mathbf{p}$<5 %.

Therefore, by using the programmable delay line, both O_C and Δ_{Oc} can be reduced to the order of ns.

4. EXPERIMENTAL TESTS

Experimental tests are developed in order to validate the correctness of the operations performed by the upgraded HI and to evaluate the time delay between two trigger signals.

The HI is equipped with a thermal compensated clock with period 100 ns.

The measurement of the time delay between the trigger signals is executed by connecting the pins RB1 of the HI#1 and HI#2 to the input channels Ch#1 and Ch#2, respectively, of the Digital Storage Oscilloscope (DSO) Tektronix TDS7154B, as shown in Figure 5.

The sampling frequency of the DSO is set to 10GS/s, to ensure a sampling period equal to 0.1 ns.

The Master PC is connected by a GPIB interface bus to the DSO, and sends the trigger conditions to the two HIs by Wi-Fi connection. In the experimental tests the trigger conditions are the same for both HIs.

The time delay between the triggers is evaluated by means of the number of samples occurring between the crossing of the established threshold by the two input signals. In particular, denoting i and j the indexes corresponding to the samples crossing the threshold, and dt the sampling period of DSO, the time delay is:

$$\Delta t = \left|\left(i - j\right) dt\right|. \quad (7)$$

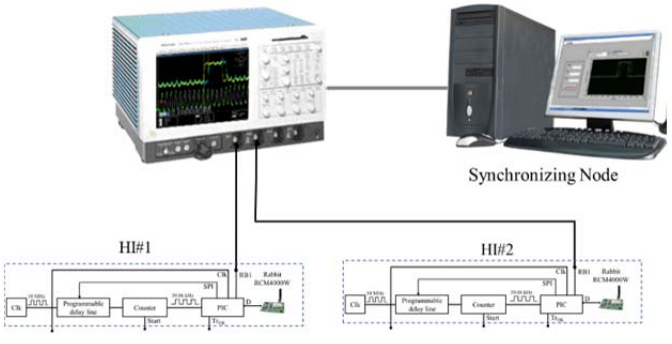

Figure 5. Experimental setup to evaluate the delay between the trigger signals generated by two HIs.

In the first set of experiments the following parameters are set: n_{itp} = 351562, n_m =4000, and ν_m = 39062. With this setup, the first trigger is generated after n_{itp}*2^8*100 ns = 9 s from the end of the HIs synchronization. This time is enough to disconnect the HIs from the Starter Block and to connect them to the MIs. The successive 4000 triggers are generated each ν_m * 2^8 * 100 ns = 1 s.

Figure 6a) shows the trend of ΔT versus the acquisition time, Figure 6b) its histogram in the case the synchronization of the two HIs is performed at the beginning and the programmable delay line is not used. In this case ΔT is characterized by the mean value μ = 62.3 ns and standard deviation σ = 0.4 ns. Similarly, Figures 6c) and 6d) show the trend of ΔT and its histogram evaluated by repeating the synchronization procedure. In this case ΔT is characterized by μ=86.1 ns and σ = 0.4 ns.

Figure 6 shows that, without the programmable delay line, the mean value of the delay between the HI triggers depends on the synchronization procedure and does not change during the observation time. In the two different experiments the widths of the variation ranges are comparable.

Figure 7a) shows the trend versus the acquisition time of ΔT, Figure 7b) its histogram in the case the synchronization of the two HIs is performed at the beginning and the programmable delay line is used. In this case ΔT is characterized by μ = 5.8 ns and σ = 0.4 ns. Similarly, Figures 7c) and d) show the trend of ΔT and its histogram evaluated by repeating the synchronization procedure. In this case ΔT is characterized by μ = 7.3 ns and σ = 0.4 ns.

These results confirm the effectiveness of the proposed synchronization procedure to compensate for Δt_{ph}.

The results of repeated experiments highlight: (i) the proper operation of the upgraded starter block makes that the delayed start of the PIC does not influence the synchronization accuracy and (ii) with the upgraded HI architecture, the delay between the trigger signals is a low percentage of the clock period of HI.

5. CONCLUSIONS

The synchronization accuracy of the Hardware Interfaces (HIs) bringing the common sense of the time to standalone MIs [1] is improved.

The HI architecture is upgraded by adding the programmable delay line after the clock in order to reduce the phase delay that is the main source degrading the synchronization accuracy.

The synchronization procedure is also upgraded to provide the measurement of the phase delay that must be compensated by adjusting the delay line.

The experimental results indicate that, by considering the actual realization of the upgraded HI, the accuracy obtained is a low percentage of the HI clock period, whereas with the previous configuration it is one clock period.

The on-going activity is devoted to developing a HI able to work in scenarios with or without networking. When the network is not available, the HI works as described in the paper. When the network is available, the HI will implement a synchronization procedure based on packet exchange.

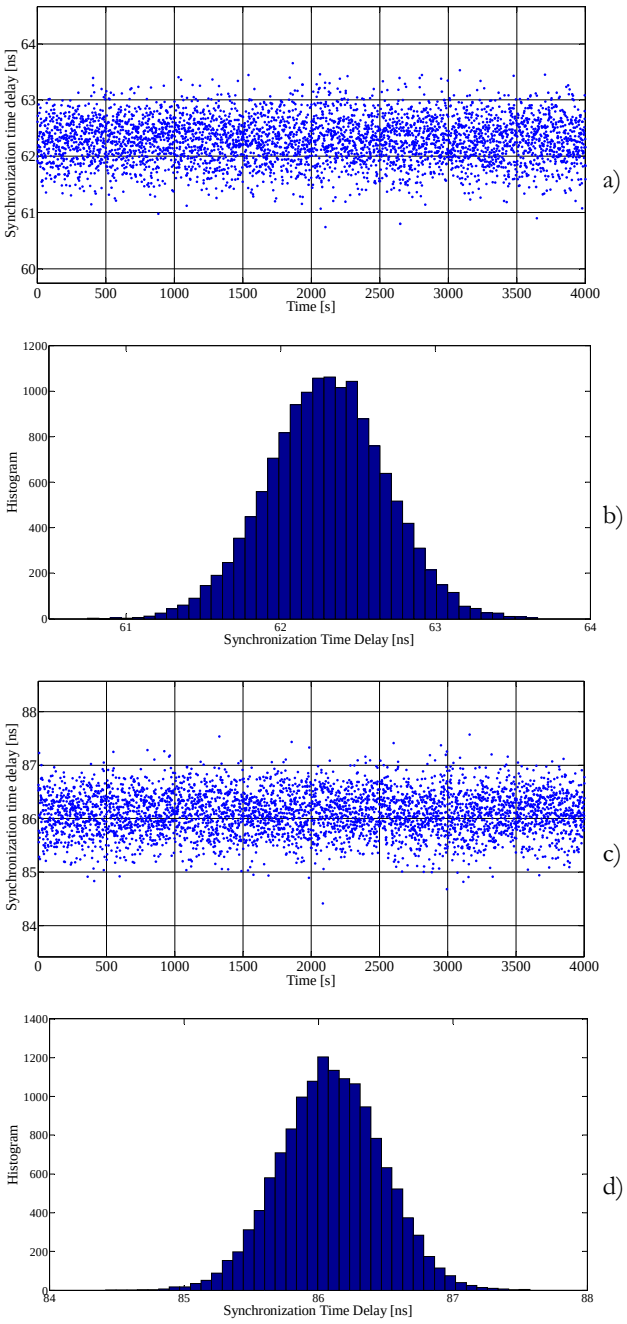

Figure 6. Trends of ΔT versus the acquisition time a), and their histogram b), in the case where the synchronization of the two HIs is performed at the beginning and the programmable delay line is not used. c) and d) are evaluated by repeating the synchronization procedure.

6. ACKNOWLEDGEMENT

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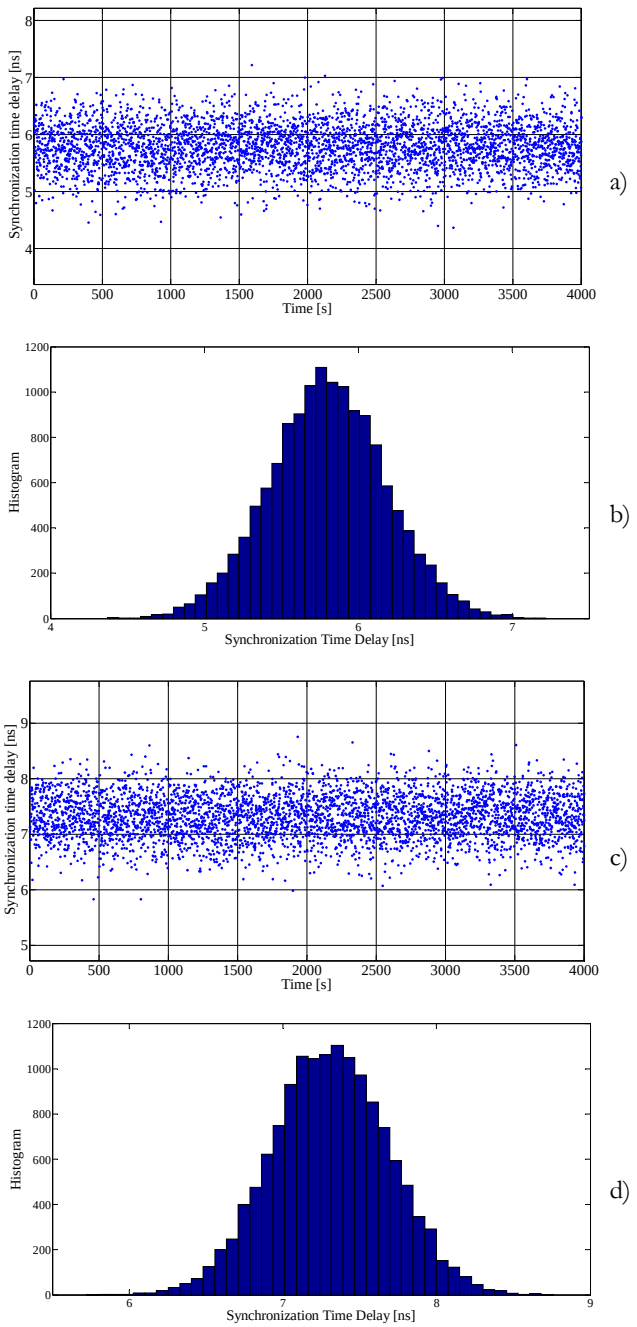

Figure 7. Trends of ΔT versus the acquisition time a), and their histogram b), in the case where the synchronization of the two HIs is performed at the beginning and the programmable delay line is used. c) and d) are evaluated by repeating the synchronization procedure.

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