

# Bandwidth limits in Hall effect-based current sensors

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## ABSTRACT

Modern power applications are demanding for small and broadband current sensors. Hall sensors are a good solution, but practical implementations are limited to a few hundred kHz. The literature offers a theoretical knowledge about the dynamic effects acting on the Hall probe but does neither define nor experimentally assess the bandwidth fundamental upper limit, since many parasitic dynamic effects perturb the inherent time response of the Hall sensor. This paper experimentally investigates the bandwidth upper limits in CMOS Hall effect-based current sensors. Based on the physics-based description of the Hall probe, the paper defines a novel, special-purpose, measurement technique, which is able to experimentally evaluate the inherent response time of the Hall probe without triggering the main parasitic effects. The paper also proposes an equivalent electrical model describing the dynamic response of the Hall probe so as to better explain and understand the measurement results. Specifically, the paper identifies two bandwidth upper limits: a fundamental limit set by the intrinsic capacitance, which models the transversal charge accumulation due to the Hall effect, and a more practical limit set by the capacitive input of the electronic readout interface. Some main parasitic effects are then assessed and added in the proposed model.

**Keywords:** Hall sensor; current sensor; silicon Hall probe; wide bandwidth; Hall sensor model

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## 1. INTRODUCTION

Current sensors are key elements in the design of a large family of power systems, such as motor drivers and power converters [1]. Modern power applications, like power management in electric vehicles, are demanding for small, or even silicon integrated, current sensors with state-of-the-art performance in terms of bandwidth, linearity, isolation, power consumption, and many other requirements [2]–[5]. Among these specifications, wide bandwidth (i.e., from DC to several MHz), together with reduced dimension, is the most challenging [1]–[3]. Broadband current sensors are usually implemented by means of either a resistive shunt or a current transformer (CT) [6], [7]. The former is relatively cost-effective but is quite bulky and realises a non-isolated measurement. At the best of our knowledge, the only CMOS-integrated resistive shunt is reported in [6], but heat dissipation is still an issue. On

the other hand, current transformers realise isolated measurements but are bulky, quite expensive and suffer from magnetic saturation.

In this framework, current sensing based on the Hall effect is very promising in terms of size, cost and power consumption, since the Hall probe can be easily integrated into a CMOS System-on-Chip (SoC): in particular, power consumption can be reduced down to just a few mW. However, practical realizations still show limited bandwidth. Commercially available CMOS-based Hall sensors are usually limited to less than 250 kHz [8]–[10]. In the literature it is possible to find some particular Hall-based solutions with a -3-dB bandwidth of 1 MHz or above, but these are either implemented by using non-standard semiconductor compounds [11] or combine the Hall element with CTs (or coils) to achieve the broadband capability, with the Hall probe still covering only the low-frequency sub-band [12].

The physics-based description of the Hall probe (i.e., the magnetic field sensitive element within the sensor) suggests three main bandwidth-limiting high-frequency phenomena: i) relaxation time of the carriers; ii) inductive effects; iii) capacitive effects [13]. The first limit (in the THz-GHz range) is due to scattering effects attempting to restore the energy equilibrium [13], and represents only a theoretical cut-off since it cannot be achieved by any practical implementation of the sensor. The second and third limits are associated with the inherent reactive behaviours shown by a real Hall probe. To these physics-based/technological effects, other architecture- and operation-related limits must be added. For instance, the well-known and commonly used spinning-current bias technique, which is devoted to offset rejection, introduces another bandwidth upper-bound, which is set by the time required by the technique to correctly sample and cancel out the offset voltage at the output of the Hall probe [14]–[16].

This paper aims at empirically investigating the bandwidth fundamental and practical limits in Hall-based current sensors, regardless of the geometry of the Hall probe as well as the specific architectural readout solution. Hence, limits due to the spinning-current technique, or other readout procedures, will not be considered. The paper exploits special-purpose experimental techniques (supported by numerical analysis) in order to assess these main bandwidth limits. An equivalent electrical model describing the dynamic response of the Hall-based current sensor is also proposed, for a better interpretation of experimental results. With the support of both physics-based description and the proposed empirical model, the paper identifies a test, which is able to experimentally demonstrate, in the time domain, that capacitive effects actually determine the two main frequency limits. Specifically, the intrinsic equivalent capacitance, which models the transversal charge accumulation occurring in the probe due to the Hall effect, defines what in the following will be addressed as the bandwidth “fundamental” limit, i.e. the theoretical bandwidth of the sensor in the case the Hall probe were interfaced with an ideal readout circuit. However, the capacitive input of the actual readout interface connected to the output of the probe sets a more “practical” bandwidth limit at lower frequencies, since it increases the total capacitance influencing the Hall probe response. In addition, several parasitic dynamic effects superimpose and further perturb the time response of the Hall sensor, degrading it with respect to the inherent RC-like time response: the modelling approach offers hints on how to take them into account.

The paper is organized as described in the following. Section 2 reviews the basic theory of the Hall effect and describes the geometrical and physical properties of the Hall probe prototype employed in this work. Section 2 also presents the proposed circuit-based equivalent model. Section 3 investigates the bandwidth limits in Hall probes by means of numerical analyses. Finally, Section 4 reports all the experimental measurements carried out to assess the bandwidth fundamental and practical limits, making also use of the model and comparing results with the discussion in the previous section. Conclusions are drawn in Section 5.

## 2. THEORY AND MODELLING

### 2.1. Hall effect and Hall probe

The Hall probe (Figure 1) is a magnetic field sensitive device relying on the well-known Hall effect. Basically, the Hall effect

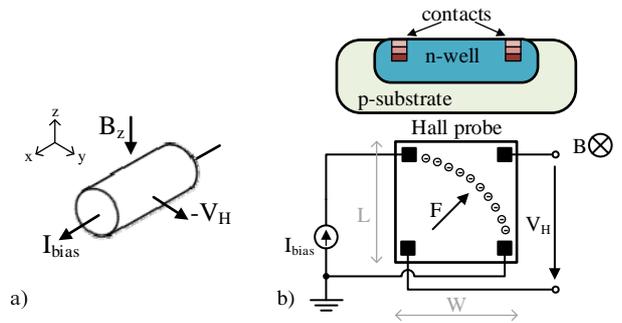


Figure 1. a) Angular relationships between electromagnetic quantities due to the Hall effect. b) Simplified cross section of the Hall probe provided by STMicroelectronics and top view of the Hall probe connected to surrounding circuits.

is a manifestation of the Lorentz force applied by an external magnetic field  $B$  to the charge carriers flowing through a material [13]. This force bends the carriers from their original path and causes a transversal accumulation of charge with an associated potential difference  $V_H$  (namely, the Hall voltage) that (in static operation) nominally follows the formula:

$$V_H = S_I \cdot I_{bias} \cdot B_Z, \quad (1)$$

where  $S_I$  is the current-related sensitivity of the Hall probe,  $I_{bias}$  is the bias current, which defines the flow of charges and their original path, and  $B_Z$  is the component of the magnetic field along the direction orthogonal to the plane on which the bias current is flowing.

The Hall probe is commonly realized by means of semiconductors, rather than metals, due to their lower charge carrier mobility [13]. In the following, we will refer to a standard square-shaped silicon Hall probe realized by a thick n-well, which constitutes the sensing area, surrounded by a lowly doped p-substrate and connected to the embedding electronic circuits via four square contacts realized by means of highly doped  $n^+$  implantations and placed at the angles of the well (Figure 1). The Hall sensors employed in this work are provided by STMicroelectronics and are realized in BCD (Bipolar-CMOS-DMOS) 0.16- $\mu\text{m}$  technology. The chosen Hall probe is only a possible and quite standard realization in CMOS technology, but many other implementations, with different geometries or even completely different structures, can be considered without affecting the fundamental results that are described in this paper, since the shape of the response time does not depend on the particular Hall probe.

The current-related sensitivity  $S_I$  depends on geometrical and physical properties. It is usually expressed as

$$S_I = G \frac{r_H}{qNt_{eff}}, \quad (2)$$

where  $G$  is a correction factor accounting for the specific geometry of the probe,  $r_H$  is the Hall scattering factor expressing the ability of the material to generate the Hall voltage,  $q$  is the elementary charge,  $N$  is the doping level of the n-well and  $t_{eff}$  is the effective thickness of the well, which takes into account the thickness reduction due to depletion region occurring at the pn-junction [17].

As defined in (1), the Hall probe is a magnetic sensor. Due to the vector formulation of the Lorentz force, there is a well-known angular relationship between the three electromagnetic quantities in (1); hence, a Hall effect-based current sensor must

be carefully realized so as to maximize the orthogonal component of the magnetic field. To this end, a copper strip is deposited  $d_{vert}$  above and  $d_{lat}$  far from the centre of the probe, as shown in Figure 2. The relationship between the sensed current  $I$  flowing into the strip and the magnitude  $B$  of the related magnetic field is given by the algebraic Biot-Savart law:

$$B = \frac{\mu_s}{2\pi r} I, \quad (3)$$

where  $r$  is the radial distance between the Hall probe and the copper strip, and  $\mu_s$  is the silicon magnetic permeability (that is almost equal to the vacuum permeability). Obviously, (3) is strictly valid only if both the copper strip and the Hall probe widths were negligible with respect to their displacement  $r$ , thus a full electromagnetic simulation is needed in practical cases, as considered in the following. Even though the realistic I-B relationship is more complicated, FEM analyses showed that it can be still considered algebraic. Hence, time variations in the measurand  $I$  instantaneously results in time variations of the orthogonal component of the magnetic field  $B_z$ .

Under static operative conditions the Hall voltage can be written in the practical case as:

$$V_H = S_I \cdot I_b \cdot f(I), \quad (4)$$

where  $f(I)$  is an algebraic function with respect to the measurand.

## 2.2. Electrical model

Starting from the considerations made in the previous subsection, we propose the three-port, parallel RC-based circuitual model of Figure 3 for the description of the Hall probe dynamic behaviour. The three ports are: i) the measurement port, i.e., the port through which the measurand  $I$  flows, ii) the bias port, for the injection of the bias current, and iii) the output port, at which the Hall voltage can be sensed. This model is in agreement with the static theory of the Hall effect

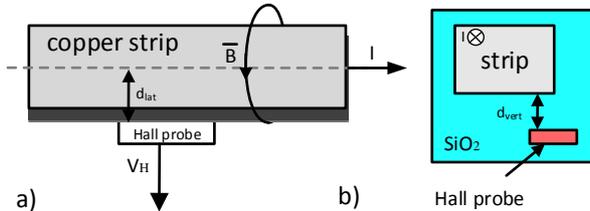


Figure 2. a) The sensed current  $I$  flows through a copper strip placed  $d_{vert}$  above and  $d_{lat}$  far from the centre of the Hall probe. b) Cross section highlighting the vertical displacement between the copper strip and Hall probe.

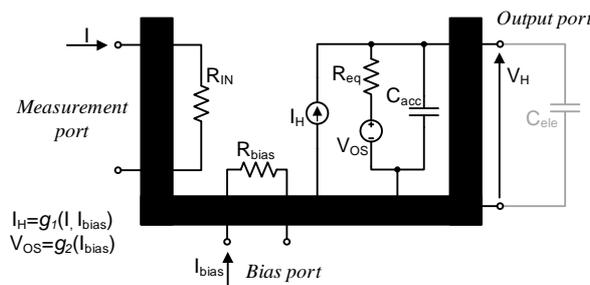


Figure 3. Three-port equivalent model of the Hall effect-based current sensor.

described above, given

$$V_H = R_{eq} I_H \quad (5)$$

$$R_{eq} = \frac{W}{L} \cdot R_{sq} \quad (6)$$

$$I_H = G \frac{L}{W} \mu_H I_{bias} \cdot f(I) = K \cdot I_{bias} \cdot f(I)$$

where  $R_{sq}$  is the square resistance of the n-well,  $L$  and  $W$  are the well sizes and  $\mu_H$  is the Hall mobility defined as  $\mu_H = \mu_N \cdot r_H$ . The equivalent resistance  $R_{eq}$  is the resistance seen between the two sensing contacts. The equivalent current  $I_H$  can be defined as the Hall current, whose AC contribution represents (under general dynamic operating conditions) the transversal local flow of carriers due to the Lorentz force. This current is modelled as a current-controlled current generator, for which the controlling parameters are both the bias current  $I_{bias}$  and the measurand  $I$ . This relationship is intuitively correct since the amount of deflected carriers depends on both the magnitude of the magnetic field (thus on the magnitude of the measurand  $I$ ) and the number of charge carriers that are flowing in the probe (thus on the magnitude of the bias current  $I_{bias}$ ). Following (5), the static Hall voltage is given by a pseudo-ohmic relation between the equivalent resistance  $R_{eq}$  and the Hall transversal current  $I_H$ . Note this is not a real ohmic relation since there is not a real transversal DC current flowing from one sense contact to the other, but it is a mere mathematical equivalent.

In dynamic operation, the Lorentz force immediately reacts to the measurand  $I$ , but the charge carriers need time to (de-)accumulate on one side of the probe in response to the time-variant Lorentz force. More precisely, the instantaneous equivalent accumulated charge shows non-negligible memory effects with respect to the force and cannot be adequately described according to a static model. This dynamic behaviour can be reasonably modelled by inserting a capacitor  $C_{acc}$  in parallel to the equivalent resistance.

It is well known that a significant DC voltage contribution is present on the output port of the Hall probe, which depends on the level of the bias current, even though no magnetic field is applied. This offset voltage  $V_{OS}$  is mainly due to technology issues that generate asymmetry in the probe and can be order of magnitude higher than the actual Hall voltage, complicating the readout process. For this reason, the offset voltage in Hall probes is extensively investigated in the literature [14], [18]–[21]. The common model for the offset in a Hall probe is an unbalanced resistive bridge. This model is fully recognized by the community but it cannot be easily implemented in our model, since the latter decouples the bias port from the output port. Hence, a voltage generator  $V_{OS}$  controlled by the bias current  $I_{bias}$  is directly placed in series to the resistance  $R_{eq}$  in Figure 3.

The other two ports of Figure 3 can be basically modelled by two simple resistors, which denote the resistance of the copper strip ( $R_{IN}$ ) and the resistance of the probe along the bias direction ( $R_{bias}$ ). Finally, all the intrinsic ports are surrounded by a global black-box that takes into account all the extrinsic parasitic physical phenomena that are not described by the intrinsic core of the model, such as induced electromotive force (EMF), magneto-resistivity, additional inductive effects, electrical coupling among the pins of the Hall probe and so on.

The capacitance  $C_{acc}$  accounts for the only one dynamic effect dealt with by the proposed intrinsic model, thus we implicitly assume that it sets the bandwidth fundamental upper

limit. This hypothesis will be validated by both simulations and measurements in the next sections. It is not easy to investigate this dynamic effect by means of common techniques, since the accurate generation of fast time-varying magnetic fields is a difficult task. In addition, fast variations of  $B$  would excite parasitic phenomena described by the black-box in Figure 3, perturbing the response of the equivalent circuit. Nevertheless, based on the physics-based description and accordingly to the proposed model, another measurement procedure able to investigate the dynamic behaviours at the output port can be identified. Since the offset voltage is due to spurious charge flow and accumulation throughout the same physical region associated with Hall accumulation, and is dependent on the bias current, then time variations of  $I_{bias}$  trigger the same RC time constant triggered by the variations of the magnetic field (i.e., of the current  $I$ ), without exciting most of the other (parasitic) dynamic effects. This particular operative condition will be exploited to experimentally characterize the RC time constant of the Hall element.

### 3. NUMERICAL SIMULATIONS

The prototype of the Hall probe, without I-B transduction, was designed to show an equivalent resistance  $R_{eq} = 3 \text{ k}\Omega$  and an intrinsic capacitance  $C_{acc}$  lower than 1 pF, accordingly to the probe description of Section 2.1 and the equivalent electrical model of Section 2.2. The probe was modelled and simulated using the physical simulator Synopsys Sentaurus Device®. This tool takes into account all the typical phenomena occurring in a semiconductor device, from carrier transport model to electron-hole recombination, carrier scattering, and mobility degradation. Moreover, the tool embeds an enhanced formulation of the current density that models the Lorentz force applied by a magnetic field  $B$  to the carriers flowing through the semiconductor:

$$\vec{J}_n = \vec{J}_0 + \frac{\mu_n}{1 + (\mu_H B)^2} \left[ \mu_H \vec{B} \times \frac{\vec{J}_0}{\mu_n} + \mu_H \vec{B} \times \left( \mu_H \vec{B} \times \frac{\vec{J}_0}{\mu_n} \right) \right], \quad (7)$$

where  $\vec{J}_0$  is the current vector due to only the applied bias. A full description of the simulation environment, together with validation of the approach by means of static analysis and a full static characterization of the Hall probe can be found in [17], [22]. For completeness purposes, Figure 5 reports the static characteristic of the Hall probe when biased with a constant DC  $I_{bias} = 500 \text{ }\mu\text{A}$  and varying the magnitude of the incident magnetic field along the z-axis from  $-50 \text{ mT}$  to  $+50 \text{ mT}$ . The figure shows a constant sensitivity of the probe of  $124 \text{ mV/T}$  with a non-linearity error of less than  $2 \text{ }\mu\text{V}$ . Even though the simulated probe is perfectly symmetric, the static simulation

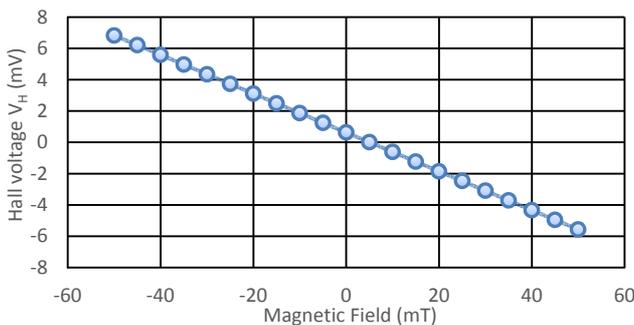


Figure 5. Simulated static characteristic of the probe.

reports an offset of less than 1 mV when no magnetic field is applied, which is due to numerical errors.

There are no particular problems in the simulation of fast magnetic fields, so standard investigation procedures of the dynamic behaviour can be realised. A 40-mT magnetic step was applied to the probe varying the capacitive load on the output port ( $C_{ele}$  in Figure 3). The simulated time-domain responses of the Hall voltage are shown in Figure 5. The probe response is quasi-static when no capacitors are coupled to the sensor (we can estimate a time constant  $\tau$  of less than 2 ns), while it shows a time constant  $\tau$  of about 18 ns when it is loaded with 6 pF (3 pF on each sense contact). The figure reports the simulation points fitted in Matlab® with spline functions.

The simulation results, where main parasitic effects have been neglected, suggest that the bandwidth upper limits of the Hall probe are defined by RC time constants [22]. Explaining these simulation results with the equivalent electrical model of Section 2.2 leads to two bandwidth limits: a fundamental limit, which is defined by the product of  $R = R_{eq}$  and the intrinsic capacitance  $C_{acc}$ , and a more practical limit that is defined by the product of  $R = R_{eq}$  and the total capacitance  $C = C_{acc} + C_{ele}$  facing to the output port. Note that the equation for  $C$  is rigorously true under the assumption that  $C_{acc}$  is directly connected to the output port. Nonetheless, in a realistic architecture  $C_{ele}$  is the differential input capacitance of amplifier stage(s) plus capacitive parasitics. Accordingly to the proposed electrical model, the time constants extracted from the above-described simulation leads to  $R_{eq} = 3 \text{ k}\Omega$  and  $C_{acc} \leq 0.7 \text{ pF}$  which are in agreement with the design values. The simulation also defines that the bandwidth fundamental upper limit for the simulated Hall probe is about 100 MHz.

Numerical simulations were also exploited to prove the novel measurement procedure that is proposed at the end of Section 2.2. The current  $I_{bias}$  acts on both the offset generator  $V_{OS}$  and the transversal current generator  $I_{1B}$ , as shown in Figure 3. Thus, it is still possible to prove the proposed measurement technique even though the offset is not modelled in the numerical simulator, since the probe is perfectly symmetric. Under a constant DC magnetic field, a step change of  $I_{bias}$  causes a step change of  $I_{1B}$ , triggering the same RC circuit triggered by a step change of the magnetic field. From a physical standpoint, a variation of the bias current changes the total sensitivity  $S_I \cdot I_{bias}$  of the Hall probe and, consequentially, the amount of accumulated charge, which must re-allocate in the probe triggering the same physical phenomena.

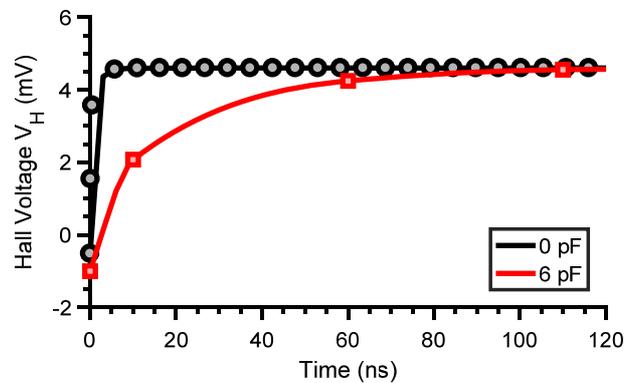


Figure 4. Simulated time response of the Hall probe to a magnetic step of 40 mT with different loading capacitances connected to the output port. The sensor is DC biased with 500  $\mu\text{A}$ . Interpreting the resulting time constants with the proposed electrical model leads to electrical parameters that are in good agreement with design values:  $R_{eq} = 3 \text{ k}\Omega$ ,  $C_{acc} < 0.7 \text{ pF}$ ,  $C_{ele} = 6 \text{ pF}$ .

Figure 6 compares the time responses of the Hall probe to a step change of magnetic field with the time response to a step change of the bias current, with no readout circuits connected (i.e.  $C_{ele} = 0$  F), demonstrating that both stimuli trigger the same dynamic behaviour. Dark circles reported in both Figure 5 and Figure 6 are the results of the same simulation, but values on the ordinate in Figure 6 are normalized to the steady-state value, so as to easily compare the two time responses.

#### 4. EXPERIMENTAL INVESTIGATION

Two batches of CMOS Hall effect-based current sensors were experimentally analysed. The Hall probe is the same in both batches, but they integrate different circuits. More precisely, *batch a* is a hybrid solution, which integrates only the Hall probe, with bias and signal conditioning implemented by off-the-shelf components (Figure 6a); while *batch b* monolithically integrates the Hall probe together with all the auxiliary circuits i.e., bias network and voltage amplifiers, into a single CMOS integrated circuit (IC) (Figure 6b). Given the implementation described above, *batch a* has obviously much

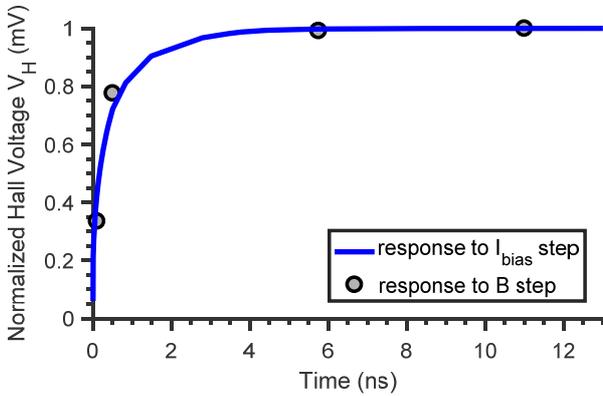


Figure 8. Simulated time response of the Hall probe to a step change of  $B$  while  $I_{bias}$  is kept constant (black circles) and simulated time response of the Hall probe to a step change of  $I_{bias}$  while  $B$  is kept constant (blue line). The Hall voltage is normalized to the stationary value so as to easily compare the kind of time response. The simulations demonstrate that both the magnetic field and the bias current trigger the same dynamic phenomena.

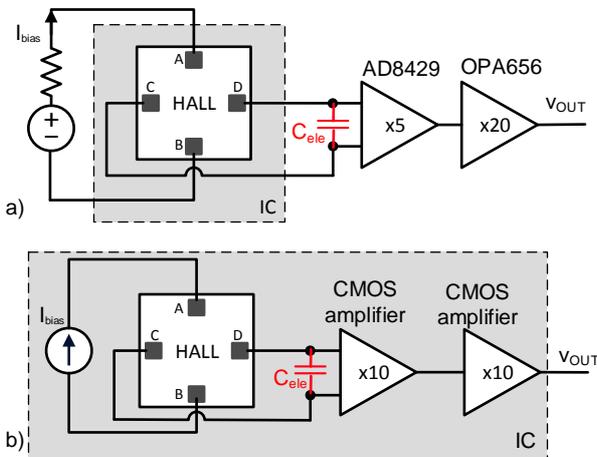


Figure 6. *Batch a*): the auxiliary circuits are external to the CMOS chip integrating the Hall effect-based current sensor. *Batch b*): both Hall effect-based current sensor and auxiliary circuits are monolithically integrated on the same substrate.

bigger load capacitance  $C_{ele}$ , in the order of several tens of pF, and it is expected to experimentally exhibit a slower time constant, while *batch b* is a solution that minimizes the value of  $C_{ele}$ . The technological parameter  $C_{acc}$  is the same for both sensors.

The analysis was based on the measurement procedure described in Section 2.2 and validated in Section 3, that consists in the measurement of the output voltage response to a step of the bias current  $I_{bias}$ . The measurement procedure was as follows: a square-wave current  $I_{bias}$  with zero mean was applied to the sensor through contacts A and B (bias port) while no current  $I$  is injected into the sensing strip (measurement port). In this way, the output voltage  $v_{OUT}$  is an amplified version of the response of the RC network of Figure 3 to a step change of the offset voltage  $V_{OS}$ , allowing the estimation of the inherent time constant of the sensor. Bandwidth limitations of the amplifiers were taken into consideration during result analysis.

An NI-PXI 5124 data acquisition board operated at 200 MSa/s with AC input coupling acquires the output voltages.

#### 4.1. Hall sensing element with external circuits

The result of the test applied to the Hall probe with external auxiliary circuits (*batch a*) is reported at the top of Figure 7. The bias current  $I_{bias}$  was generated off-chip by applying a square-wave voltage on a resistor connected in series to the Hall probe. This hybrid setup is affected by parasitic and coupling effects. In particular, the high bumps shown in Figure 7(top) are due to parasitic capacitive coupling between bias port (nodes A and B) and output port (nodes C and D); this coupling is mainly due to the particular pin-out of the chip (i.e. pins connected to the bias port are close to pins connected to the output port). Although the output voltage suffers from high bumps at the beginning of the step response, the expected exponential response is clearly visible. From this result it is possible to estimate a time constant  $\tau = (200 \pm 40)$  ns and a  $-3$ -dB bandwidth of  $(800 \pm 200)$  kHz, which, accordingly to the proposed model, leads to  $C = (66 \pm 12)$  pF given  $R_{eq} = 3$  k $\Omega$ . This is a reasonable value for a hybrid system made by discrete components.

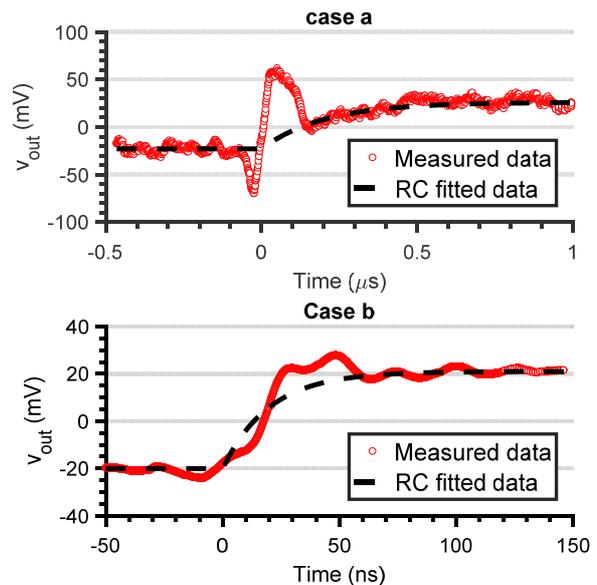


Figure 7. Measured response to a step change of  $I_{bias}$ , giving insights into the inherent RC time response for both batches of sensors. Parameters extracted from the measurements are: *batch a*)  $R=3$  k $\Omega$ ,  $C=66$  pF; *batch b*)  $R=3$  k $\Omega$ ,  $C=4$  pF.

## 4.2. Hall sensing element with integrated circuits

The step response of the Hall probe integrated with conditioning circuits (batch *b*) is shown at the bottom of Figure 7. The bias current  $I_{bias}$  is now generated on-chip by means of a high-compliance current mirror. Also in this case, the measured voltage is not a pure exponential function since there are other residual dynamic effects acting on the response (e.g., the residual capacitive coupling between contacts and the ringing of the amplifiers which are underdamped second order systems). However, by fitting the output voltage with an exponential function it is possible to estimate an inherent time constant  $\tau = (12 \pm 3)$  ns, after de-embedding 4 ns as time response for each CMOS amplifier stage (which have 40 MHz bandwidth). The estimated time constant leads to a total capacitance  $C = (4 \pm 1)$  pF, which is in good agreement with the numerically estimated values of  $C_{acc} = 0.7$  pF and  $C_{elc} = 2$  pF (those parameters are extracted from actual architecture and layout of the system). Since batch *b* minimizes the value of  $C_{elc}$ , this test identifies the bandwidth practical upper limit of the Hall sensor prototype, which is between 9 and 18 MHz.

In conclusion, both tests were carried out in correspondence with operative conditions that activate a few parasitic dynamic effects, while the inherent parallel RC is fully excited. The experimentally obtained values for time constant and capacitance  $C$ , both for the implementation in which the capacitive load is maximized (batch *a*) and for the case in which such a load is minimized (batch *b*), are in agreement with numerical analysis, thus validating the model shown in Figure 3 and confirming that the bandwidth upper limits are set by the parallel RC circuit. Parasitic dynamic effects are superimposed to such a fundamental response, and they degrade the actual bandwidth, as investigated in subsection 4.4.

## 4.3. Analysis in the frequency domain

Frequency analyses were performed on both batches to further investigate the dynamic response of the Hall probe. In this test, no current  $I$  was applied to the strip, hence  $v_{OUT}$  is an amplified version of the thermal noise generated by the Hall probe and the output amplifiers, only. The voltages were recorded by the NI-PXI5124 board at 12-bit resolution and 100-MSa/s sampling frequency. Then, noise power spectrum densities (PSDs) were estimated in Matlab® using the Welch algorithm (Flat Top window with 4096-long segments and 90 % overlap between segments [23]). The measured DC – 50 MHz output power spectra  $S_{OUT}$  are shown in Figure 9.

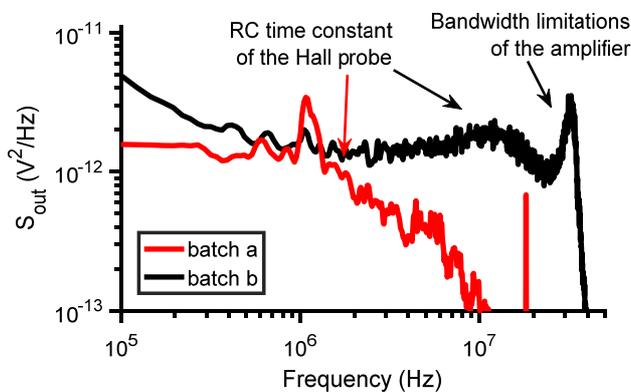


Figure 9. Measured noise power spectrum densities of  $v_{out}$  for both batches when no current  $I$  is applied to the copper strip. The power spectra confirm that the bandwidth practical upper limit is defined by the RC time constant where the  $C$  is mainly due to the capacitive load of the readout electronics.

Although the PSDs cannot be interpreted, strictly speaking, as the frequency response of the entire current-measuring system, nonetheless interesting information can be derived by observing their shapes: more precisely, it is possible to identify two important points in the noise PSD of batch *b* (black line): a first cut-off frequency around 15 MHz and a second cut-off frequency around 40 MHz. The former relates to a time constant of nearly 10 ns, in agreement with the RC time constant of the Hall probe measured in Section 4.2, while the latter relates to the bandwidth limitation of the output amplifiers. This noise PSD confirms the result of the time-domain test obtained in Section 4.2. On the contrary, the noise PSD of batch *a* (red line) shows a single cut-off frequency, between 1 and 2 MHz, and then a typical  $-20$ -dB roll off. This cut-off frequency corresponds to an estimated time constant between 80 and 160 ns, in line with the time constant estimation from the time-domain test of Section 4.1.

The noise PSD of batch *a* shows a cut-off at frequencies lower than what was reported by the noise PSD of batch *b*, confirming all the above discussed theory. Since the dynamic performance is mainly defined by the RC time constant, the higher capacitive load, which is due to the external electronic readout, slows down the time response of batch *a* with respect to batch *b*. The cut-off frequency of batch *a* is approximately one order of magnitude lower than the cut-off frequency of batch *b*, in agreement with time-domain tests reported in Sections 4.1 and 4.2.

## 4.4. Time response to actual magnetic transitions

The batch *b* was tested also in the presence of an actual fast (but not instantaneous) time transition of magnetic excitation. In this test the Hall element is DC biased, i.e. the current  $I_{bias}$  is kept constant so that output dynamics are related only to changes of the magnetic field. We designed a simple voltage-to-current (V/I) converter based on a voltage follower and a  $1\text{-}\Omega$  power resistor (Figure 10). The generated time-varying current  $i(t)$  is monitored by means of the voltage drop across the power resistor, and then it flows through the metal strip on the top of the Hall probe, generating the desired transition in the magnetic field  $B$ . The designed V/I converter is characterized by a rise time of 210 ns, short but one order of magnitude longer than the practical response time estimated in Sections 4.2 and 4.3. Hence, the Hall probe, as described by the model of Figure 3, works in the quasi-static regime as far as the parallel RC is concerned. However, the parasitic dynamic effects described by the black-box are now fully triggered and will degrade the voltage response. This experiment provides useful information about these parasitic dynamic effects embedding the core of the sensor behaviour.

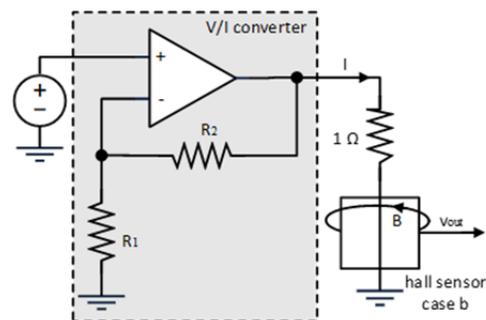


Figure 10. Measurement setup for time response to magnetic step.

We acquired the voltage across the power resistor, translated it into the current  $i(t)$  and fed it into the model of Figure 3 implemented in SPICE. The first version of the model takes into account the parallel RC core only, without any element in the black-box. The predicted output voltage  $\tilde{v}_{OUT}$  is then compared to the measured output voltage  $v_{OUT}$ . The voltage  $\tilde{v}_{OUT}$  (Figure 11, solid blue line) shows a quasi-instantaneous response to the measured current stimulus (top of Figure 11), as expected, but does not fit measurement data (red circle), since the model neglects parasitic effects. Specifically,  $\tilde{v}_{OUT}$  does not foresee the high bump opposite to the exponential transition. This mainly because the model still does not describe the parasitic EMFs induced by time-varying magnetic induction (which must be modelled in the black box). In fact, when the model is made more realistic by inserting proper inductive equivalent elements in order to take into account parasitic EMFs, then the predicted voltage (solid black line) accurately fits the measured data. In this case, the effect of parasitic EMFs is well fitted by adding a transformer to the model, as shown by the refined model of Figure 12. The primary winding is placed in series to  $R_{IN}$  in the measurement port while the secondary winding is connected in series to the RC core (secondary winding being 180 degrees rotated). The measurand  $i(t)$  flows into the measurement port generating an inductive effect on the output port that opposes the transversal Hall current  $I_H$ .

This test, when compared with that of Figure 7 (bottom),

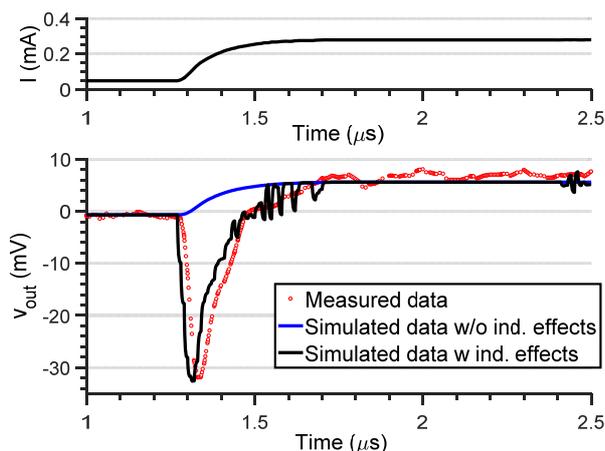


Figure 11. Measured response (red dots) to a step change of  $I$  (batch of case b) compared with the simulated response given by the core model of Figure 3 (blue line) and with the simulated response given by the enhanced model of Figure 12 with inductive transformer (black line). Parameters used for the simulation are  $R=3\text{ k}\Omega$ ,  $C=4\text{ pF}$ ,  $L_{\text{prim}}=10\text{ nH}$ ,  $L_{\text{sec}}=30\text{ nH}$ .

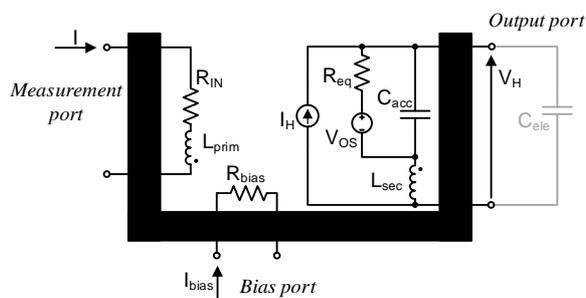


Figure 12. Modified three-port equivalent model with the insertion of a transformer between measurement port and output port so as to take into account the parasitic EMF generation.

shows an example of the degradation of the inherent RC time response when parasitic effects are triggered in realistic operation of the sensor. Suitable design methodologies must be employed in order to minimize the deviation from the practical bandwidth limit. For example, since the induced EMFs are strictly related to the layout design of the implemented prototype, they can be reduced by proper geometrical redesign (e.g., minimizing the area described by connections from the sensor to amplifiers).

## 5. CONCLUSIONS

This paper experimentally investigated the bandwidth upper limits in Hall effect-based current sensing. To this end, an ad-hoc measurement technique, which was derived from both a physics-based description of the Hall effect and an equivalent electrical model, was proposed and exploited. The test was performed on two different batches of sensors, with the same Hall probe but different capacitive loads. The proposed electrical model allowed better interpretation of the measurement results giving insights on the underlying phenomena. According to the equivalent electrical model, the experimental tests demonstrated that the intrinsic capacitance  $C_{acc}$  which models the charge accumulation occurring in the probe due to the Hall effect, defines the fundamental upper bandwidth limit of the Hall-based current sensor. This fundamental limit degrades to a more practical limit (placed at lower frequencies) due to the unavoidable capacitive load added by the readout circuit. These results fully agree with numerical simulations and frequency-domain measurements, both reported in this manuscript.

A real-operation test was performed on one of the two batches, showing that the actual time response of the Hall sensor is degraded by parasitic dynamic effects. Hence, suitable design methodologies are needed to achieve the fundamental time response. One of the parasitic effects degrading the sensor response, i.e. the generation of electromotive forces due to time-variant magnetic fields, has been investigated and an extension to the original model, which takes such effect into account, has been proposed.

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