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The implementation of FPGA for data transmission between ADC and DSP peripherals in the measurement channels for power quality assessment

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ABSTRACT
The paper presents the FPGA Xilinx Spartan 3 series implementation in an analog data acquisition system, in particular consisting of nine ADCs and the TigerSHARC DSP processor. Because of different standards of ADC and DSP data interfaces, the exchange of data between them requires the use of an intermediary device for combining their communication ports. The procedures for sending data from the ADC to the FPGA buffers, their conversion and subsequent transmission to the TigerSHARC DSP are described. The digital representations of ADC analog input signals are sent to the FPGA through three lines of serial interface at the physical layer compatible with the SPI standard. After processing in the FPGA they are sent to the DSP, with the four-line interface in the LVDS standard. The paper discusses the properties of related interfaces, standards, procedures and control of ADC issues as well as the algorithms of the FPGA configuration program and functions implemented in this system. Selected results of functional testing are shown.

Keywords: ADC; DSP; FPGA; interface; electrical power quality

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1. INTRODUCTION

On-line analysis of power quality in an electrical power system is associated with the need for fast acquisition and processing of data collected from the tested system. The power quality analyzers offered for this purpose enable the determination of multiple parameters. Unfortunately, usually it is not specified according to which algorithms they are operating and what standards are the basis for their calculation. For example, we have indicated a few different definitions of the THD (Total Harmonic Distortion) coefficient, concerning estimation of waveform distortions [1], a few definitions of voltage imbalance [2, 3] and some approaches related to power theories [4]. In addition, the measurement results obtained with various kinds of analyzers in some cases seem to differ substantially.

The Department of Marine Electrical Power Engineering of Gdynia Maritime University undertook a research project to develop an estimator/analyzer of power quality in which the relevant parameters are determined in accordance with the standards [2, 4, 5, 6 and 7]. One of the key points of this development is focused on implementation of the FPGA (Field Programmable Gate Array) for data transmission between ADC (Analog-to-Digital Converter) and DSP (Digital Signal Processing) peripherals in the measuring channels of the considered device.

The paper is organized as follows. Firstly, the main ideas concerning on-line analysis of power quality in an electrical power system and its association with fast acquisition and processing of data collected from the tested system are briefly presented.

In section 2, the measurement channels are shown and discussed based on a case study – the estimator/analyzer of power quality developed, constructed and tested at Gdynia Maritime University. The lack of compatibility between ADC output interfaces and used DSP communication ports was a reason to introduce an appropriate FPGA module as an intermediate device.

In section 3 the ADC and DSP communication features are analyzed, in the context of the AD7656 converter and the TigerSHARC processor as applied devices. The conversion process and data acquisition procedures, signals and parameters are presented.

In section 4, firstly, the scope of selected FPGA implementations is discussed, and secondly, the features of FPGA applied in the chain ADC-FPGA-DSP and considered configuration program algorithms are described in detail.

Next, section 5 is devoted to the fundamental tests of measurement channels carried out in the estimator/analyzer for power quality. Firstly, three steps of the examination of the concept of the FPGA device, concerning simulation in the WebPACK Design Software environment, the functional tests of communication correctness and the estimator/analyzer functional tests are presented. Secondly, three kinds of the last functional tests related to voltage quality parameters monitoring, current and power parameters analysis and maximal SPI SCLK frequency setting are shown.

Finally, the conclusions and indications for future activity are collected in section 6.

2. MEASUREMENT CHANNELS CONFIGURATION

Measurement tracks (Figure 1) of signals from the power system contain typical input circuits including a set of voltage dividers, galvanic separation systems and anti-aliasing filters. The voltage signals are fed to the inputs of ADCs of type AD7656 (Analog Devices). A single AD7656 chip contains six ADCs.

Determination of the individual parameter values for assessment of the electrical power quality takes place in the DSP processor ADSP TS-201 TigerSHARC (Analog Devices).

The DSP processor communicates with external systems via a custom protocol Link Port, using 128-bit data frames and the LVDS interface. DSP has no native support for the SPI protocol. On the other hand, the AD7656 chip has high speed parallel and serial interfaces, allowing the data to be exchanged with external devices.

Due to the lack of compatibility between ADC output interfaces and the DSP communication port, i.e. Link Port, the FPGA Spartan 3 (Xilinx) was used as an intermediate device. Besides providing communication between ADC and the DSP system the FPGA device also mediates the exchange of information with the GPP (General Purpose Processor) LPC3250 microcontroller (ARM926EJ-S core) (Figure 1), which implements the user interface features, such as support for the keyboard, graphic display, transmission via USB and Ethernet ports.

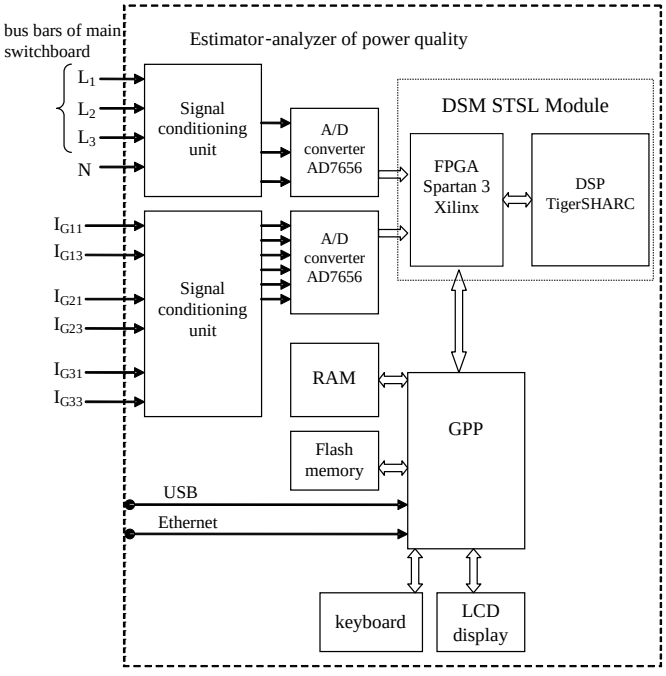


Figure 1. The measurement channels configuration of the developed estimator/analyzer.

3. ADC AND DSP COMMUNICATION FEATURES

The AD7656 chip contains six 16-bit, low power, fast, successive approximation ADCs [8]. The AD7656 has throughput rates up to 250 kS/s. It can accommodate true bipolar input signals in the ±4×VREF range and ±2×VREF range. The AD7656 also contains an on-chip 2.5 V reference (Figure 2).

The conversion process and data acquisition are controlled from the external device using CONVST signals (Figure 3) and an internal oscillator. Three CONVST lines (CONVST A, CONVST B, and CONVST C) allow independent sampling of the three ADC pairs (channels 1-2, 3-4 and 5-6). The rising edge of CONVST initiates simultaneous conversions on the selected ADCs. The conversion time is 3µs. When the conversion is complete, the signal on the BUSY output goes low to indicate that the conversion results, stored in the output data registers, are ready for readout. A simultaneous sample of all six ADCs can be performed by connecting all three CONVST A, B, C pins together.

The AD7656 is equipped with two types of data output interfaces: parallel and serial. The selection of the type of interface was preceded by an analysis of the features of both interfaces. In the designed application (Figure 1) nine ADC channels, i.e. two AD7656, were applied, so in parallel output connection of both circuits, beside BUSY and CONVST lines, 33 lines (2x 16 data lines + 1 control line (_RD)) have to be used. In serial connection, the data output needs only 7 lines (2x3 data lines + 1 clock line (SCLK)).

The parallel interface t_{ACQ} acquisition time (Figure 3), i.e. time required to output all six 16-bit words (from V1 to V6) from ADC registers, is about 700 ns. On the other hand, the serial interface t_{ACQ} acquisition time is about 943 ns, as will be explained in the next Section, which is sufficient according to the project assumption.

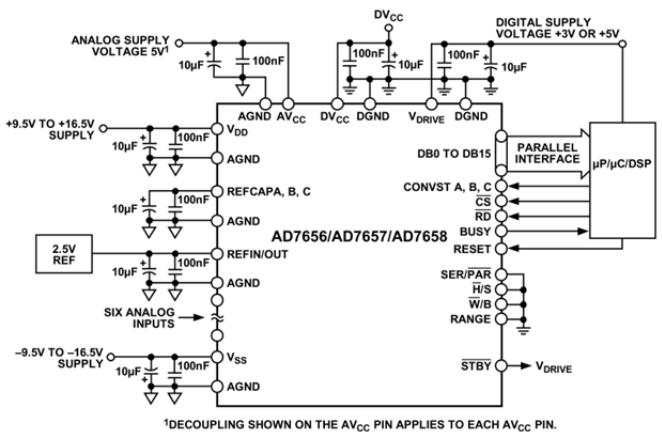


Figure 2. The configuration of AD7656 [8].

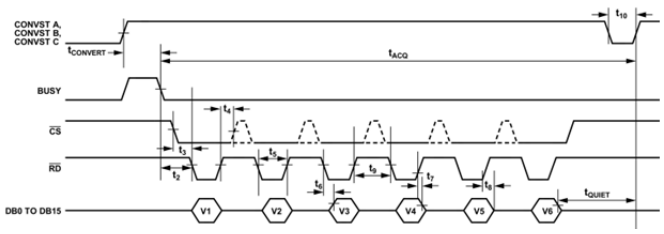


Figure 3. The ADC registers data output procedures through the parallel interface [8].

Taking into account the complicity of ADC output connection lines as well as the timing of data outputting, the serial interfaces of AD7656 were selected. Then only 7 interface lines instead of 33 are necessary for ADC data access.

The three-line serial interface applied in the AD7656 chip is compatible with the standard one-line SPI serial interface [8, 9]. Data transfer is synchronized with a rising or falling edge clock (depending on the configuration), and their set-up on the slope opposite to the sending data. The SCLK frequency used for control of data transfer can reach a few MHz, depending on a given application. Figure 4 shows the signals in the SPI lines.

In the serial interface mode of AD7656 three DOUT pins (Figure 5), DOUT A, DOUT B, and DOUT C, are available. Data can be read out from the ADC using one, two, or all three DOUT lines. Figure 5 shows six simultaneous conversions and the read sequence using three DOUT lines. Also in Figure 5, 32 SCLK transfers are used to access the data from all six registers of the AD7656; however, two sets of 16 SCLK individually framed transfers can also be used to access the data.

The TigerSHARC [10, 11] is a 128-bit processor, designed to perform operations on floating-point and fixed-point numbers, bearing the double sets of ALU units for both types of operation, the internal memory of 24Mb DRAM, integrated circuits I/O, 14 channels of DMA, and 4 internal buses for fast exchange of data between memory and the peripheral circuits and other CPUs. Because of its features, it is a very suitable DSP for designation of power quality parameters.

The TigerSHARC processor has four full-duplex type Link Port circuits that can operate in parallel. These ports use in the physical layer the interface LVDS (Low Voltage Differential Signal) [12], in which the information (in 128-bit frames) is sent using a low voltage differential signal in the symmetrical copper cables in the system loop. The LVDS protocol enables data transmission speeds of up to 4 Gb/s with very low power consumption. Each Link Port can be configured to exchange data on one or four interface lines. Figure 6 shows the interface line configuration and signals in the LVDS interface.

As mentioned above, the two interface standards differ significantly and the only way to provide the data exchange

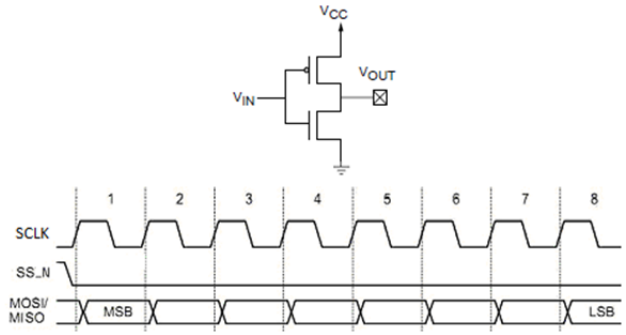


Figure 4. The line driver and waveforms in the SPI interface lines.

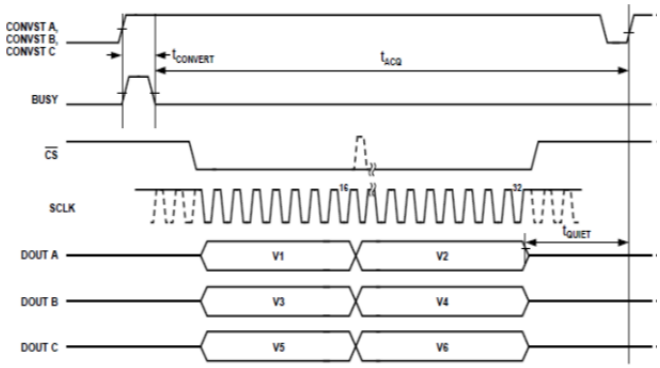


Figure 5. The signals in the AD7656 serial interface lines [8].

between ADC and DSP is to apply an intermediate device.

4. FPGA FEATURES AND CONFIGURATION PROGRAM ALGORITHMS

The need for high speed data processing in many applications is becoming more and more common. The multi-channel measurements as well as the high sampling rate of the ADCs demand the use of advanced acquisition techniques. The features of the current FPGAs make them especially suitable to act as an interface between the set of high speed ADCs and DSP. They can be adapted to different ADCs or different DSP interfaces. The next advantage is the possibility to shift some tasks, usually performed in the DSP, to the FPGA implementation. It lowers the load on the DSP and often speeds up the execution of certain operations. Some examples related to selected FPGA implementations can be found in [13, 14, 15 and 16].

In the designed system the FPGA XCS1000 Xilinx Spartan 3 [17, 18] was used, to provide the acquisition in the TigerSHARC of data obtained from AD7656. In Figure 7, the interface connections of the FPGA circuit to the ADC and DSP devices are shown. Attached digits indicate the number of data lines in the respective bus.

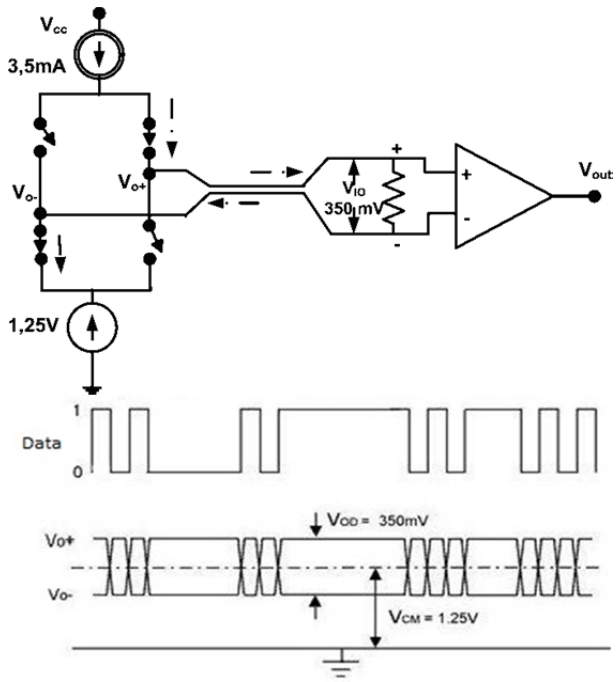


Figure 6. The configuration and signals in the LVDS interface lines [11].

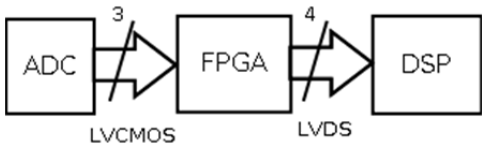


Figure 7. ADC and DSP interface buses in the measurement track.

The FPGA is a large-scale integration system, used to create high-speed digital circuits for specialized logic functions. The power consumption of these systems is much smaller than for standard digital systems and processor devices. For these systems, as for processors, the change of the implemented function requires software changes to the FPGA. The I/O lines can be configured by software to work with different voltage standards. The analog voltage comparators can act as differential input/output [17].

In general, the configuration program organizes the connection network among selected circuits of the FPGA and then the device works autonomously as every hardware device. In the considered project the basic task fulfilled by the FPGA is the conversion between different physical layer standards of the ADC and TigerSHARC interfaces as well as different formats of frames transmitted by both links.

For handling of the ADC SPI interface, the respective FPGA lines were configured as LVCMOS25 and for TigerSHARC as LVDS_25 (Figure 7). The output data from the ADC are available at one time on three lines DOUT A, B, C (Figure 5, Figure 8). On the 1st line the ADC conversion results are transmitted in sequence from input channels 1 and 2, on the 2nd line from channels 3 and 4, and on the 3rd line data from channels 5 and 6. The transfer of all data requires 32 SPI SCLK cycles, but in case only three channels are needed and when the input signals are connected to the channel inputs 1, 3 and 5, to transfer such data only 16 SPI SCLK transfers are necessary. When the SPI SCLK frequency is equal to 16 MHz the transfer of three 16-bit words from the ADC takes approximately 943 ns. The A/D conversion takes about 3 μs, so the full ADC conversion cycle and output of digital data requires about 3.95μs, which means the maximal frequency of A/D operations is above 253 kS/s (Figure 8). Such a result is possible because other operations performed in the FPGA, connected with data transmission to the TigerSHARC, are implemented parallel in time with the next A/D conversion cycle. The data from three FPGA buffers BUF have to be overwritten to eight RAM blocks (this takes about 480 ns), because of the configuration of the four-line LVDS interface connecting the FPGA with the TigerSHARC Link Port. The transmission through the Link Port requires approximately 160 ns.

The time dependencies shown in Figure 8 illustrate the location of individual operations during the A/D conversion cycle. More explanations of the procedures implemented in the FPGA are presented in the algorithm in Figure 9. The conversion cycle begins every 4 μs with CONVST going high, generated in the FPGA. After the digital data in cycle n of the conversion are completed and the ADC line BUSY goes low, the FPGA clock SPI SCLK starts pulling data V1, V3 and V5 (16-bit words) from DOUT registers (in the ADC) to the BUF buffers (in FPGA). After 16 cycles the SPI SCLK clock stops and data are shifted from three BUF to eight RAM. Then the state of the output line ACK from the TigerSHARC is examined. If it is high, the FPGA issues 100 MHz clock managing data transfer from the FPGA RAM to the TigerSHARC on four differential lines of the LVDS interface.

The operations performed in the FPGA during the A/D conversion (BUSY at high state) take less than 1 μs. They are performed in parallel with other A/D operations in the next A/D cycle; otherwise it would not be possible to obtain the assumed frequency of the A/D conversion.

In Figure 10, the configuration of functional blocks developed in the FPGA to establish communication between the AD7656 and the TigerSHARC DSP is shown. The individual functions are performed sequentially, under control of the "stanu" signal (Figure 10). The sequential algorithm provides correct flow of operations and elimination of the phenomenon of hazard between digital signals, unwanted pulses as well as the possibility of suspension of the device. As was previously described, the sequence of operations starts with the CONV signal, generated in the FPGA every 4 μs, then the FPGA is waiting for the BUSY signal. The next operations in

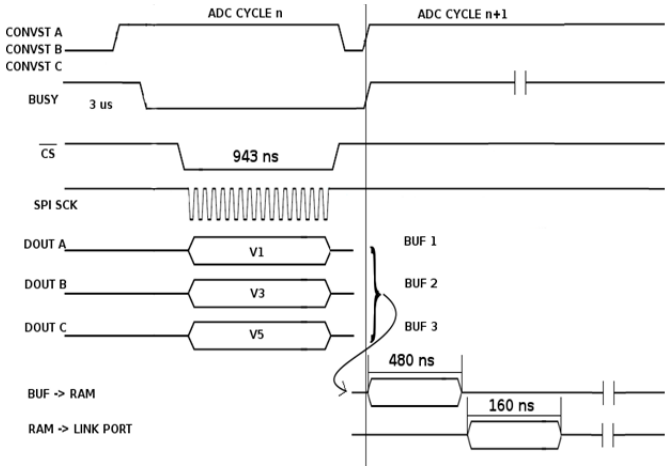


Figure 8. ADC data handling during A/D conversion.

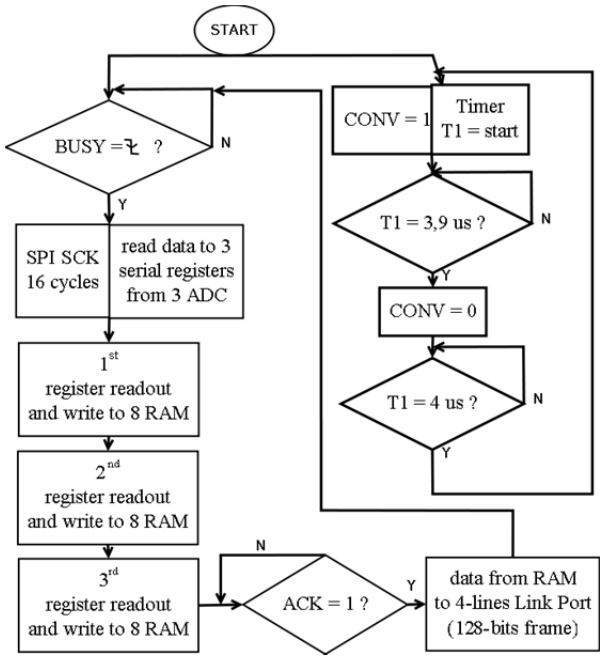


Figure 9. Algorithms performed in the FPGA.

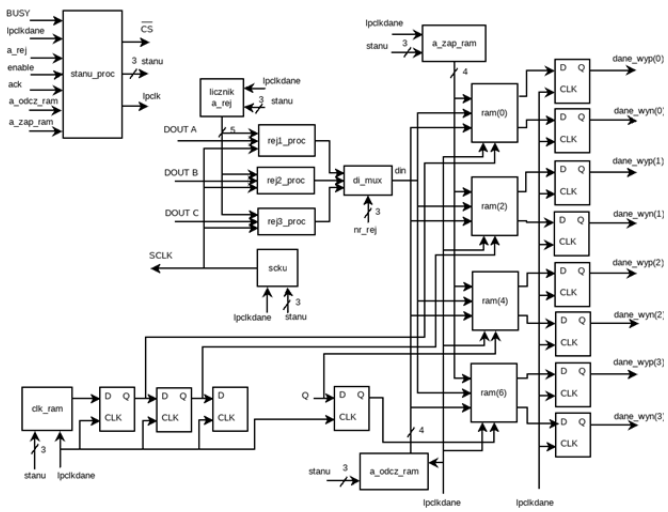


Figure 10. The structure of the functional blocks configured in the FPGA.

sequence are performed autonomously, under control of the FPGA internal clocks. Finally, the data transfer to the DSP begins when the ACK signal from the Link Port enables start of transmission, also under control of the FPGA clocks.

5. FUNCTIONAL TESTS

The examination of correctness of the accepted concept of the FPGA device was performed in 3 stages:
- the simulations in the WebPACK Design Software (Xilinx) environment while designing the FPGA configuration program (Figure 11),
- the functional tests of communication correctness; the ADC input was fed with the signal generated in the Agilent 33220A Function Generator and digital samples in TigerSHARC memory were observed (Figure 12) also as a waveform,
- the estimator/analyzer functional tests (Figure 13).

The Xilinx WebPACK FPGA programming environment is a tool for configuring internal structures of the FPGA as well as enabling one to perform simulations for verifying correctness of process signals on selected functional blocks in the FPGA (Figure 10). Part of the simulation window is shown in Figure 11. The satisfactory results of simulations gave the final configuration of functional blocks implemented in the FPGA and proper sequence of operations connected with data transfer from ADC to DSP.
The examination of functionality of the structures configured in the FPGA was carried out for real input signals from the Agilent 33220A Waveform Generator. The input signals were at

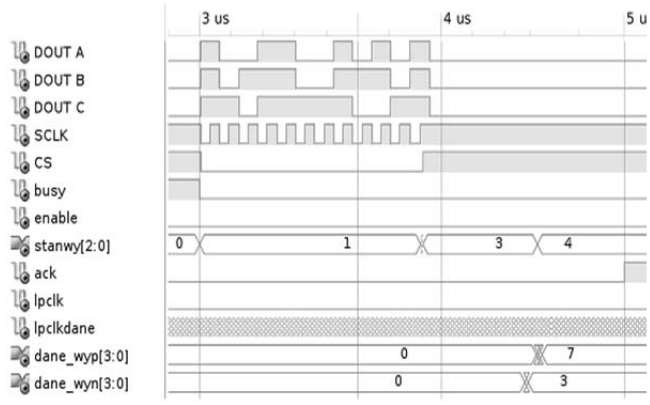
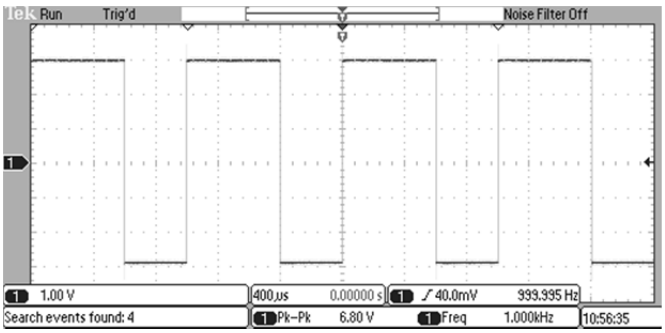
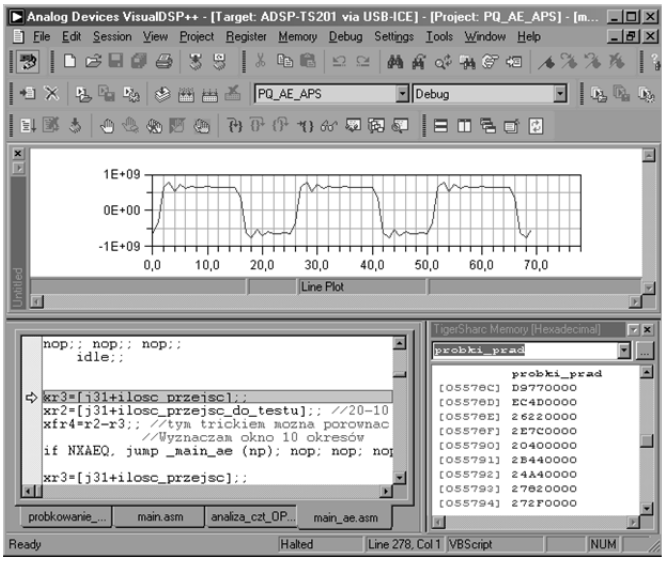


Figure 11. The simulations in the WebPACK environment.



a)



b)

Figure 12. The exemplary results of communication correctness tests: a) the input signal, b) the samples acquired in TigerSHARC memory and the respective waveform plotted in the VisualDSP++ environment.

the same time registered with a Tektronix MSO 2024 Oscilloscope (Figure 12a). Figure 12a presents an exemplary square wave with a frequency of 1 kHz and V_{pp}=6V. The samples of the input signal were converted in the ADC and their digital representations were transmitted via the FPGA to DSP memory. In Figure 12b, the window of the test program is shown. The application in DSP in the VisualDSP++ (Analog Devices) environment contains the exemplary data collected in the DSP in hexadecimal code as well as the respective waveform for the input signal as in Figure 12a. The cut-off frequency of anti-aliasing filters in the measurement channel during this test was set at 10 kHz.
The examination was performed for various signals, with different frequencies and amplitudes. The observed results ensured the correctness of data transmission via the FPGA and confirmed that no transmitted sample was lost.

The developed estimator/analyzer of electric power quality gives some options of the device for choice by the user. These options [19] concern a kind of analysis (voltage quality monitoring or monitoring of power/current distribution), mode of operation (estimator/analyzer), and also a kind of power system and number of generators working in parallel. As was mentioned, the instrument can operate in two basic modes: estimator and analyzer. In the first mode, only the parameters whose current values exceed user-defined limits are determined, whereas in the latter mode all defined parameters are calculated [19]. Starting with the option "voltage quality monitoring", we

Table 1. Measurement of voltage quality parameters. Exemplary test results for phase L1.

	f = var		δ
	PXI NI	E/A	%
U_{rms} /V	220.6	220.3	0.15
U_1 /V	219.7	219.4	0.15
THD %	8.84	8.81	0.34
U_5 /V	5.01	5.00	0.20

can choose "estimator mode" as well as "analyzer mode". Choosing the option "power and current load distribution" is possible only in "analyzer" mode.

For the functional tests of the measurement channel, the three-phase power signal generator Chroma Programmable AC Source Model 6590 was used (Figure 13).

The performed functional tests among others consisted of generating signals with known harmonic content in three phase voltage. This allows the evaluation of correctness of calculations of some parameters processed in the TigerSHARC DSP. Some selected results of voltage quality parameter measurements are shown in Table 1. These are exemplary results for the L1 phase. The values of U_{rms}, U_1, THD and U_5 averaged for 150 s, i.e. 750 measurement windows, are determined for a known test signal. The δ factor represents the relative deviation between the quantity measured by means of the tested instrument and the reference value obtained from the PXI National Instruments device. It should be strongly underlined that presented measurement results are only an illustration of the functional tests of the channel under consideration for the verification of operations performed in the FPGA during A/D conversion, together with the FPGA-DSP link.

The designed implementation of the measurement channel in "estimator mode" allows the data to be acquired from three ADCs at 250 kS/s from each, as was assumed at the start of the project.

The algorithms described above concern the "estimator mode" for voltage quality monitoring. The second mode of instrument operation is "analyzer", dedicated to assessment of the proportional distribution of currents and powers. Then the A/D conversions are performed in different conditions, and the required A/D frequency is 25 kS/s only, so all processes connected with ADC data handling, performed in the FPGA, are not critical as in "estimator mode".

The tests carried out confirmed the correctness of the used algorithms and procedures applied in the FPGA device. The accuracy of determining the related coefficients is satisfactory from a practical point of view. A more detailed description and analysis of the measurement tests of the designed power quality estimator/analyzer are beyond the concept and scope of the presented paper.

Other tests were connected with maximal SPI SCLK frequency. This signal is generated in the FPGA. It causes output of ready data from ADC registers to FPGA buffers. In the technical data of the AD7656 the maximal transmission frequency is given as 18 MHz [8]. After numerous experiments the SPI SCLK frequency was set equal to 16 MHz. Frequencies higher than 17 MHz caused distortion, especially at the first bits of data words.

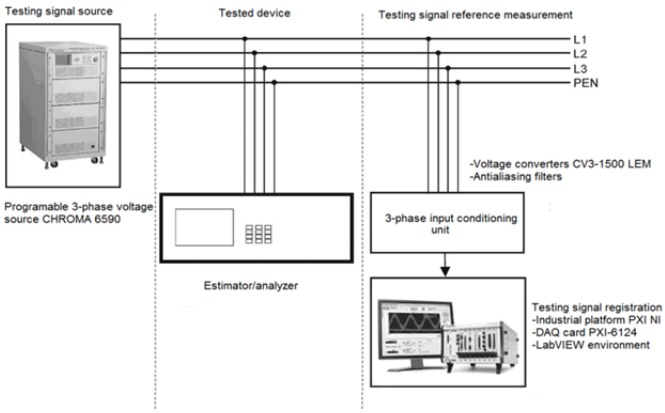


Figure 13. Laboratory stand for experimental verification of the elaborated estimator/analyzer of power quality (version 2.0) based on the appropriately defined testing signals – voltage quality parameters.

6. FINAL REMARKS

In this paper, the analysis of the given ADC and DSP interfaces was carried out. An analysis of ADC set readout timing for various interfaces and the selection of the interface type for implementation in the instrument were performed. The verification of correctness of the implemented solutions for a lossless data flow between ADCs and the DSP was carried out in a few steps, at various levels of instrument functionality.

In the designed instrument the configured FPGA fulfills many functions, sometimes critical for all instrument operation. The adaptation of data in the FPGA to enable communication between ADC and DSP includes:

— different speed of transmission; the ADC output bit transmission speed is 16 Mb/s (common three lines – 48 Mb/s), while the DSP Link Port speed is 200 Mb/s (common four-line speed is 800 Mb/s),

— different data frame formats; the single ADC output frame consists of 8 bits, while the DSP Link Port communication frame consists of 128 bits,

— different data transmitting signal standards; ADC data carrying signals are LVCMOS25 standard, while DSP Link Port signals are LVDS_25 standard.

The implementation of functions connected with data conversion using conventional discrete digital circuits (TTL or even CMOS) entails a much higher demand for power supply.

The operations performed in the FPGA are crucial to the operation of the entire measurement channel. The operations performed in the FPGA enable the efficient delivery of measurement data to the DSP.

The results of tests carried out for measurement channels in the developed estimator/analyzer of power quality confirm the correctness of the applied solutions.

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