Low-cost implementation and characterisation of an active phasor data concentrator

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ABSTRACT

The main components of an advanced measurement system based on synchrophasor technology for the monitoring of power systems are the phasor measurement unit (PMU), which represents the 'sensor', and the phasor data concentrator (PDC), which collects the data forwarded by PMUs installed on the field. For the purpose of extending the benefit of synchrophasor technology from transmission grids to distribution networks, different projects are seeking to use low-cost platforms to design devices with PMU functionalities. In this perspective, in order to achieve a complete synchrophasor-based measurement architecture based on low-cost technologies, this work presents a PDC design based on a low-cost platform. Despite the simplicity of the considered hardware, advanced PDC functionalities and innovative control logics are implemented in the prototype. The proposed device is characterised by several experimental tests aimed at assessing its performance in terms of both time synchronisation and capability of managing several PMU data streams. The feasibility of some additional functionalities and control logics is evaluated in the context of different possible scenarios.

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1. INTRODUCTION

The main components of the synchronised distributed measurement systems used in power network monitoring systems that are based on synchrophasor technology are phasor measurement units (PMUs) and phasor data concentrators (PDCs) [1]-[4]. The PMU is the 'sensor' of this measurement system and gives several measurements: synchronised phasor magnitude and phase angle; frequency; and rate of change of frequency (ROCOF), evaluated based on voltage and current signals [1]-[3]. All the measurements are time tagged using an absolute time reference in coordinated universal time (UTC) format and usually provided by the global positioning system (GPS). Measurements are encapsulated in data packets that are compliant with standard [2] and forwarded to the PDC. The data coming from PMUs in the field is thus collected by the PDC, aligned with the same timestamp and typically forwarded in suitable streams to the upper levels of the architecture (either a higher level PDC or the control centre). Different target applications, running either online or offline, can be implemented based on such data.

Synchrophasor technology was originally designed for wide-area monitoring systems (WAMSs) used in transmission systems [5]. Currently, commercial PDCs suitable for WAMSs allow for the management of hundreds of incoming streams, and their cost is in the order of thousands of dollars. These devices can implement mathematical functions (power calculations and evaluations of sequence components) and other utility functions, such as alarms, that are specific for electric substations [6]. However, such equipment is not usually programmable by users for specific functions.

Nowadays, research is pushing to extend the benefits of synchronised measurements to distribution networks. Due to the different scales and economic constraints of the two kinds of systems, ongoing industrial and academic research projects have recently been working on the exploitation of low-cost architectures for the evaluation of electrical quantities in PMU-like devices [7]-[13] and in power quality metres [14], [15].

A PMU project based on low-cost hardware can be developed using the most common single-board computer (SBC) platforms. Thanks to the low cost, good performance, and availability of the various hardware equipment that can be integrated into the boards (as wireless and wired communication), these devices are

pushing the development of prototypes that are specifically designed for different applications in IoT architectures [16].

Considering that the PDC is the first element of the synchrophasor system with a global view of an entire portion of the electric system and thanks to measurement data received from different locations in the field [17], the PDC could be engineered as a new measurement device that is able to make decisions that rely on the information received from different sources.

In [18], an active low-cost PDC that is suitable for distribution networks and is based on the most common SBC, the Raspberry Pi [19], is presented and characterised in terms of synchronisation accuracy (provided by the global navigation satellite system [GNSS] receiver) and computational burden (in terms of the number of manageable data streams). The PDC allows for the implementation of advanced functionalities and, in particular, time-related measurements, which enable advanced stream management as in [17].

In this paper, the design of the SBC-based PDC is expanded upon in order to implement a control logic relying on measurement data processing and digital output. A synchronised calibrator is used to test a complete measurement and control chain in a real scenario, in which the PDC relies on a simple frequency change detection to trigger its digital output. An overall delay characterisation is performed to show the relationship between measurement device configuration, input data latency, and processing time.

2. A PDC WITH CONTROL CAPABILITY

In a typical synchrophasor monitoring system, a commercial PDC is generally implemented as a physical device that is specifically designed to operate in an electrical substation. However, PDC functionality can also be implemented as a software tool [20] that is generally installed at the top of the synchrophasor hierarchy in the control centre of the grid operators.

As well as the functionalities of aligning and forwarding the data streams with the same timestamp, the PDC can implement additional functionalities. In the guide for PDC requirements [4], the ability to implement control logic is not specified as a functional requirement; rather, it is recommended as an additional optional function. In this context, the PDC uses the data provided by the PMU in real time and can become a crucial element not only for WAMS applications that are based on the synchrophasor measurements, but also for the wide-area monitoring protection and control system (WAMPAC).

In particular, the PDC can monitor the behaviour of the underlying measurement system, evaluating and tracking performance indices as, for example, the mean latency of each input stream. It can include specific outputs, similar to digital interfaces operating in a supervisory control and data acquisition system or an energy management system (EMS) [4].

The PDC can thus support advanced monitoring applications, and it might implement the logic for event detection as part of protection and control. In [21], the architecture of a PDC that plays an important role in a WAMPAC vision is described. In [22], a synchrophasor system with a single level of PDCs, which can manage variable input reporting rates, is introduced. In [23], a PDC specific for the real-time state estimation application is presented.

3. THE PROPOSED ARCHITECTURE

The proposed architecture is based on two low-cost hardware devices and on a software application designed in the LabVIEW environment. The cost of the overall hardware is less than € 80. Figure 1 shows the main blocks of the proposed active PDC prototype based on a SBC Raspberry Pi 3B and Uputronics synchronisation board.

3.1. Hardware

The active PDC prototype is developed using the low-cost SBC Raspberry Pi (Figure 2), produced by the Raspberry Pi Foundation [19]. The model 3B has been used here, equipped with a System on Chip (SOC) BCM2837 with a CPU quad-core ARM up to 1.2 GHz and 1 GB of RAM. The SBC is also equipped with 10/100 Ethernet and 2.4 GHz Wi-Fi 802.11n modules, which make the device able to receive the streams provided by the PMUs. A 40 pins General Purpose Input/Output (GPIO) is used to communicate with the peripherals and to generate the digital signal shown in the subsequent section. The device does not comprise a real-time clock, but, for the implementation of the active functionalities defined in [17], an accurate time reference is necessary to correctly evaluate the latency of the data packets received from each connected PMU. To overcome this lack, the prototype is equipped with a Uputronics GPS expansion board that includes a GNSS receiver. The GPS receiver has been chosen for timekeeping due to its availability and low price [24]. The U-Blox MAX-M8Q module can provide the absolute time reference pulse per second signal (PPS) with an accuracy of ± 60 ns. Generally, when the PDC cannot rely on the timestamps provided by a PMU because of the lack of synchronisation (the SYNC bit set in the data frame header), the PDC discards all the data frames for that PMU [25]. Instead, during a loss of the GPS signal feeding the active PDC, the prototype can still operate as a data concentrator using the timestamps inside the received data packets to the alignment and forwarding process. During this interval, the latency evaluation of the input data stream is suspended until the restoration of a good GPS signal.
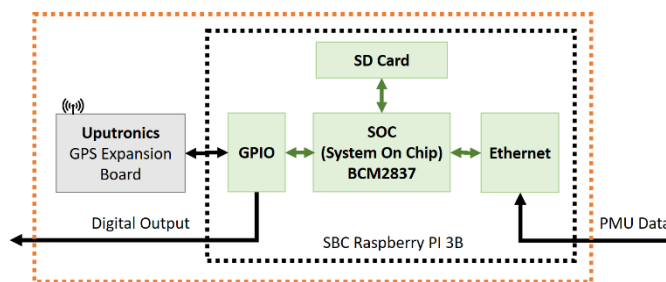

Figure 1. Proposed active PDC prototype based on SBC Raspberry Pi 3B and Uputronics synchronisation board.
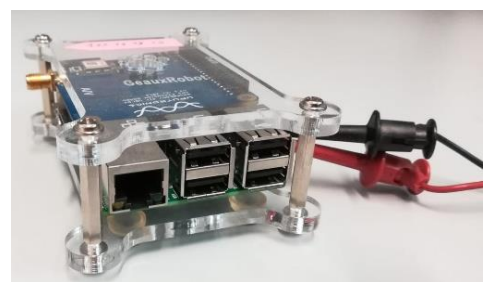

Figure 2. Hardware details of the proposed active PDC prototype (SBC Raspberry Pi 3B and Uputronics synchronisation board).
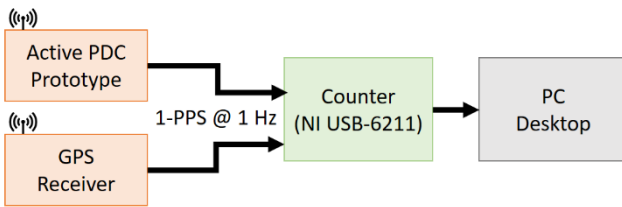
Figure 3. Experimental setup designed to evaluate the synchronisation performance of the active PDC prototype.

3.2. Software

The operating system used in the SBC is the Linux Raspbian, based on Debian. The software of the proposed active PDC is developed in the LabVIEW environment in an external PC before being installed in the low-cost board. Communication between the development PC and the LabVIEW project running in the prototype is managed by the hardware abstraction layer provided by the LINX firmware installed in the SBC. The virtual instrument (VI) running in the SBC exploits the LINX firmware that provides the necessary logic to access the SBC and GPIO interfaces [26].

4. CHARACTERISATION OF THE PDC PROTOTYPE

To validate the feasibility of the proposed approach, the performance of the prototype is firstly characterised by means of a suitable controlled test setup and two different test sections. The first one concerns the capability to evaluate the latency of the incoming data streams and the associated accuracy level. The second testing stage is focused on the performance of the prototype while dealing with multiple incoming data streams. In this case, the CPU utilisation level of the SBC is used as a performance index

4.1. Tests on time synchronisation

A good level of time synchronisation is a prerequisite to evaluate the latency of every incoming stream. The synchronisation is provided by the GPS receiver to give the Network Time Protocol (NTP)-PPS discipline to the entire system. The basic version of NTP daemon supplied on the Raspberry Pi does not support the PPS signals in the standard version, and it is thus necessary to recompile the module. The operating system is synchronised with the UTC by means of the NTP daemon (running locally on a loopback port) synchronised with the PPS signals from the GPS receiver. In this way, accurate time information can be obtained during the time characterisation test. The proposed PDC, provided with latency evaluation functionality, reads the time-tag included in every data
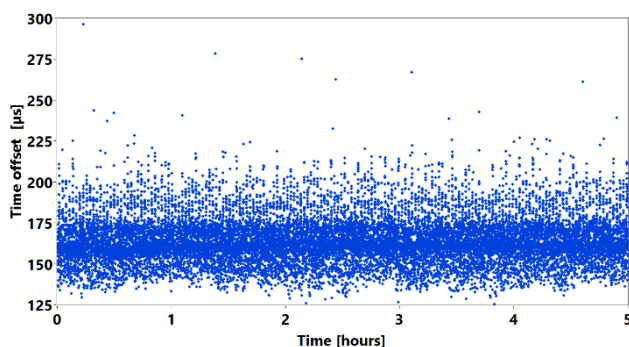

Figure 4. Time offset between the active PDC prototype and GPS receiver.
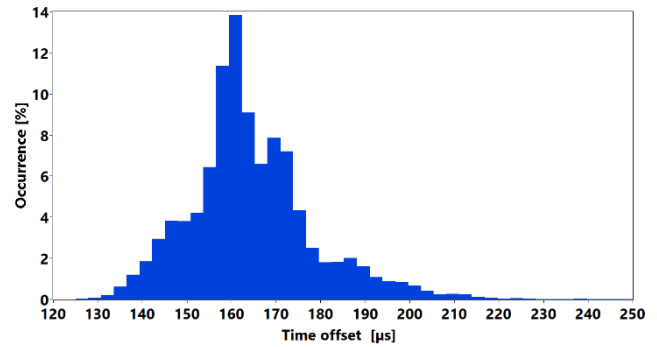

Figure 5. Histogram of the time offset between the PPS generated by the active PDC prototype and that of the GPS receiver (5 h measurements).

packet (in the SOC and FRACSEC fields of the IEEE C37.118.2 data frame header) of the incoming PMU streams and evaluates the delay between it and the arrival time of the data packet. This approach requires that the arrival time is measured with a sufficient accuracy, and a suitable source of synchronisation is therefore needed for the PDC time base [17].

Figure 3 shows the test setup for evaluating the accuracy of the time synchronisation of the prototype.

The test setup is composed of a GPS receiver Symmetricom XL-750, able to generate a synchronisation time signal of up to 50 PPS with an accuracy of ± 100 ns. The PDC prototype is programmed to generate a digital signal every second using the GPIO of the SBC. This digital signal is generated to verify the pace keeping of the occurrence of the UTC second. The GPS receiver is a reliable solution when the time coordination is difficult and when the network topology does not provide a continuous, reliable, and stable link that is either wired or wireless [27].

The two synchronisation signals (from the GPS receiver and from the prototype) are acquired, and the time offset is evaluated using the counter functionality of the National Instruments DAQ board USB-6211, which is connected to a PC desktop via USB.

Figure 4 shows the time offset measured over five hours, taking into account the 18,000 measurements corresponding to second occurrences. The distribution of the time offset is shown in Figure 5: The mean value is 164.4 μs, and the standard deviation is 14.1 μs. The maximum offset obtained in the test is 297.4 μs, and the jitter, defined as the difference between maximum and minimum time offset, is 170.7 μs.

In this test, the time offset is directly obtained by comparing the PPS signals, and no correction has been added. Nevertheless, it is clear from the results that a compensation of the average time offset would be effective in reducing the synchronisation error. This can be done by adjusting the generation trigger in the LabVIEW application. In any case, the synchronisation level obtained by the prototype is fully adequate for evaluating the latency of a PMU data stream, as reported in [3], where a 2 ms time accuracy is required.

4.2. Tests on CPU utilisation

Figure 6 represents the test setup for evaluating the performance of the PDC prototype in terms of CPU utilisation with ten incoming data streams. The data of the different streams is individually collected and evaluated in terms of latency. During this test, no other operations run in the PDC prototype. The PMUs simulator, which relies on a PMU data stream simulator software developed in LabVIEW, can generate data streams that
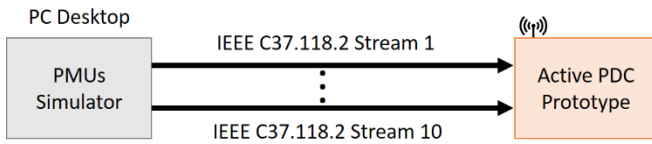
Figure 6. Experimental setup designed to evaluate the CPU utilisation of the active PDC prototype, with ten streams from the simulated PMUs.

Figure 7. Experimental setup designed to evaluate synchrophasor data latency with the active PDC prototype.

are compliant with [2], with different reporting rates. The TCP communication is used between the PMUs simulator and the PDC prototype. The PMUs simulator runs in a PC desktop that is synchronised by the local-area NTP every 15 minutes, and its clock is also used to countercheck for possible anomalous behaviour during tests.

Table 1 reports the results in terms of the average CPU utilisation (at five-minute observation intervals) and the data rate. Ten streams and different reporting rates up to 50 fps are considered. It is clear that the prototype can easily manage ten streams up to the maximum reporting rate prescribed by [1], which is 50 fps for a system operating at the nominal frequency of 50 Hz.

5. PROTOTYPE BEHAVIOUR IN A REAL SCENARIO

In the second step of the validation procedure, the PDC prototype is included in real synchrophasor architectures based on two commercial PMUs that are compliant with the last version of synchrophasor standard [3]. Another PDC is also included with the aim of evaluating the overall latency of the synchrophasor monitoring system while varying the architecture and considering the latency contributions for each component.

Furthermore, a protection logic based on the monitored quantities provided by a PMU without a digital interface is developed and implemented in the prototype of the active PDC. The last part of this section shows the results relevant to this logic.

5.1. Synchrophasor test scenarios

In the test scenarios, two network topologies are considered. In the first one, the commercial PMUs are connected to the PDC prototype by means of a commercial Ethernet switch, using the IEEE C37.118.2-2011 communication protocol encapsulated in a TPC transport layer (Figure 7). In the second test scenario, a computer with PDC functionalities is connected between the

PMUs and the PDC prototype using two different Ethernet 10/100 interfaces in order to emulate a more complex synchrophasor architecture (Figure 8).

In the first test scenario, the PDC prototype is configured to collect and evaluate the PMU latency for two incoming streams of measurement data provided by two commercial PMUs (Figure 7).

Each element of this architecture is synchronised with the UTC so that the PDC prototype can evaluate the synchrophasor data latency. including both PMU and network latencies.

The limits of PMU latency (the so-called PMU reporting latency) given in [3] are reported in 0The latency value is associated with the measurement process of the devices and strictly depends on two main PMU characteristics: the performance class and the reporting rate.

The PMUs are directly connected to the PDC by means of a 10/100 commercial Ethernet switch in a laboratory test setup without other types of network traffic. The protocol used for the characterisation is the IEEE C37.118.2-2011, which is specifically used for synchrophasor communication in power systems. The synchrophasor data latency reported in the following section is evaluated as the time difference between the arrival time of each data packet measured by the PDC (thanks to the time synchronisation functionality developed in the prototype) and the time tag included in the corresponding frame sent by the PMU.

The results of the synchrophasor data latency evaluation over 1,000 TCP messages are shown in Table 3 and Table 4 for reporting rates (F_s) of 10 fps and 50 fps (i.e. the minimum and maximum mandatory values prescribed in [1]) respectively. The

Table 1. Values of average CPU utilisation and data rates with ten incoming streams of PMU data and different reporting rates.

Reporting Rate (Fs) in fps	Data rate in kb/s	CPU Utilisation in %
1	7	6
10	70	9
25	175	15
50	351	23

Table 2. Maximum PMUs reporting latency in [3]: Fs is the reporting rate expressed in frames per second (fps)

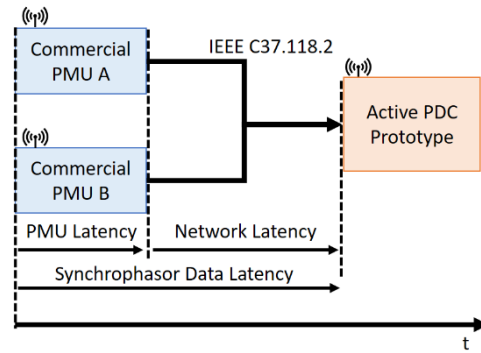| Performance Class	Maximum PMU reporting Latency in s
P	2/Fs
M	7/Fs

Table 3. Evaluation of the synchrophasor data latency (Fs = 10 fps).

PMU		Max in ms	Mean in ms	St. Dev. in ms	Limit of PRL in ms
PMU A	P	66.7	66.2	0.2	200
	M	583.4	582.7	0.2	700
PMU B	P	73.8	73.2	0.1	200
	M	718.2	713.4	0.2	700

Table 4. Evaluation of the synchrophasor data latency (Fs = 50 fps).

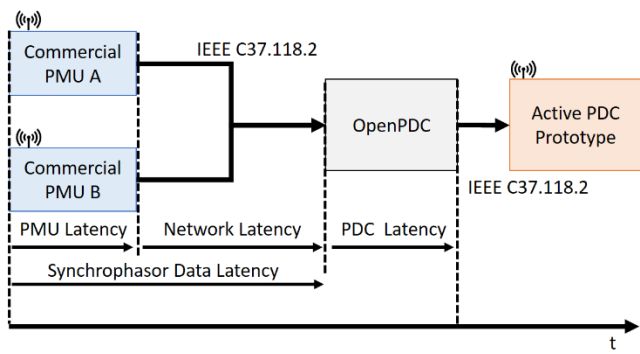| PMU		Max in ms	Mean in ms	St. Dev. in ms	Limit of PRL in ms
PMU A	P	71.0	70.5	0.1	40
	M	134.9	134.8	0.1	140
PMU B	P	73.4	73.0	0.1	40
	M	168.0	167.0	0.1	140

Figure 8. Experimental setup designed to evaluate the PDC reporting latency of the WAMS.

tables report the results for both performance classes in terms of the maximum and mean values and standard deviations. The tables also report the PMU reporting latency (PRL) limits for the different considered cases. It is important to highlight that the PRL does not consider the network latency introduced by the network devices between the PMUs and the PDC prototype, and it gives only an indication of the latency associated with the first step of measurement architecture.

It is worth recalling that the P-class is specific to applications that require low latency, and its accuracy requirements do not significantly change for the used reporting rates. For this reason, in the implementation, the same algorithm is adopted by manufacturers, and this situation leads to two very similar latency results, as indicated by the experiment results.

On the contrary, the requirements for the M-class are different for each reporting rate, and the latency values largely increase with lower reporting rates, as shown in Table 3 and Table 4.

The second test scenario is based on a synchrophasor architecture comprising two PMUs and an intermediate PDC layer (Figure 8). The commercial PMUs send their outputs to a workstation, which is equipped with an I7 quad-core Intel processor, 8 GB ram, Windows 7 operating system, and OpenPDC software [20]. OpenPDC implements the PDC functionality of collecting, aligning, and forwarding, in a single output stream, the received input data to the low-cost PDC, following the hierarchical architecture suggested in [2]. The aim of the test is to evaluate the capability of the active PDC prototype to receive data not only from commercial PMUs but also from other devices of the synchrophasor architecture, in order to verify the feasibility of the proposal.

The workstation is equipped with two Ethernet interfaces: The first one is connected to a switch in order to receive the incoming PMU streams, while the second one is directly connected by means of an Ethernet cable to the PDC prototype. Since the PMUs are connected to the unsynchronised OpenPDC system, the PDC prototype is responsible for evaluating the overall latency of the input stream, which practically corresponds to the output latency of the intermediate PDC. Comparing these

new results with those of the previous test case, it is possible to evaluate the latency generated by the intermediate PDC.

Table 5 reports the latency measurements over 1,000 TCP messages when either the P- or M-class is considered for both PMUs and with reporting rates of 10 fps and 50 fps.

The maximum latency is similar for the two performance classes. This may be attributed to the OpenPDC software, whose default configuration includes a one-second waiting time (lag time) before transmitting the aligned data. Any data arriving after that interval has elapsed is considered as late and is discarded. It is clear from the results that PDC configurations can play a crucial role in overall system performance. The above OpenPDC configuration is useful for sending data within a fixed time frame, but it strongly affects the propagation through the system layers. If measurements are used for fast response applications, then this configuration may render the benefits of the P-class PMUs useless in terms of speed. The proposed synchronised PDC proves a valuable tool for evaluating the operating conditions of complex architectures in real time.

5.2. Latency evaluation in a protection application scenario

This test scenario (Figure 9) aims to verify the performance of an application implemented in the PDC prototype and thus to test the feasibility of the PDC as an intelligent device that can send commands or protection signals. As mentioned above, the PDC prototype can evaluate the measurements contained in the data packets provided by the PMUs to implement different logics based on the input data and thus on the actual state of the electric grid. The GPIO interface is used in this test to send a digital control signal in reaction to an input variation.

The Omicron CMC 256plus synchronised calibrator [28], used specifically for test protection and measurement devices of class 0.2, is utilised to estimate the time difference between the occurrence of an electrical event and the activation of a digital output signal provided by the PDC. In this context, the calibrator generates a synchronised three-phase voltage signal used as input
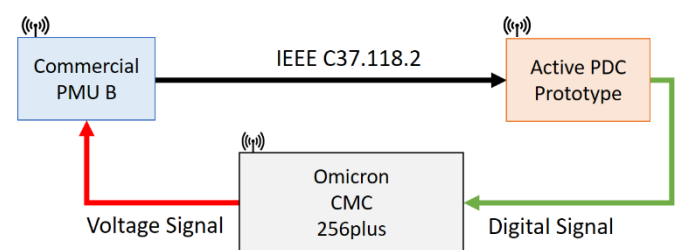
Figure 9. Experimental setup designed for the protection application scenarios.
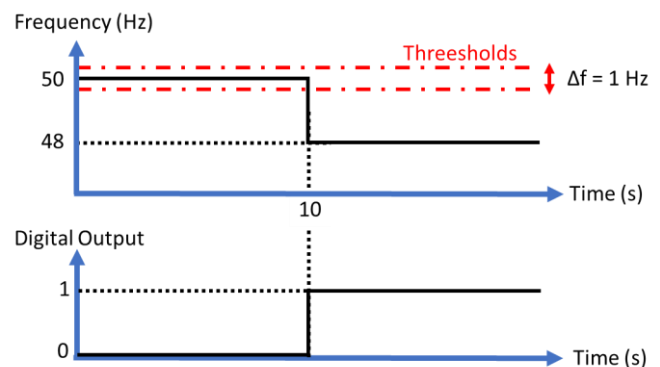
Figure 10. Frequency signal test and digital signal output.

Table 5. Evaluation of the latency with an intermediate PDC.

Fs in fps	Input streams type	Max in ms	Mean in ms	St. Dev. in ms
10	P	1015.4	1012.6	0.4
	M	1001.3	998.8	0.4
50	P	1013.8	1009.5	0.4
	M	1024.2	999.7	0.4

to a commercial PMU. It is also able to receive binary input signals, with a time resolution of 100 µs and a time stamp accuracy of ±0.00015 % of reading ± 70 µs [28]. The test voltage magnitudes (controlled by using the Omicron Power Quality Signal Generator) are 50 Vrms, and the frequency evolution is represented in Figure 10. From $t = 0$ s to $t = 10$ s, the test signal is characterised by a nominal 50 Hz system frequency, while a -2 Hz frequency step change occurs at $t = 10$ s. The commercial PMU follows the variation of the frequency and sends the measured frequency to the PDC in data packets at regular intervals. Following this configuration, the PDC prototype is programmed to check all the packets provided by the PMU and to set the digital output to a high level when the frequency variation exceeds a given threshold, which is equal here to ±0.5 Hz. The GPIO interface of the PDC is connected to the binary input of the synchronised calibrator that, thanks to the time synchronisation provided by the GPS receiver, can evaluate the time difference between the generated event (frequency step change) and the status change of the PDC digital output (low-to-high transition).

The PMU used in the test is fully compliant with [3], without a digital interface. The device is connected to the PDC prototype with a high-performance Ethernet switch, used specifically for industrial application (the switch is not reported in the figure). 0reports the maximum, mean, and standard deviation values of the data latency evaluated by the PDC prototype over 1,000 data packets for four different configurations. The results are compliant with the specification of standard [3] (summarised in Table 2).

To highlight how different configurations of the PMU can influence the detection of an event by the PDC, the tests have been performed by generating the same electrical event and using the PMU with the two different compliance classes (P- and M-classes) and two different reporting rates. It should be recalled that high reporting rates allow evaluating dynamic events in an electrical system, but they also require a PDC capable of handling the streams without increasing overall latency.

Table 7 shows the results of the overall delay of the protection application in ten different tests, each obtained for all the configurations. It should be noted that the overall delay results are close to the latency results in Table 6.

With the M-class and the lowest reporting rate, the delay between the detection of the event and the binary events reaches the highest value. Increasing the reporting rate while keeping the class, the delay is lower. This change is due to the reduced value of the synchrophasor data latency in the input of the PDC as shown in Table 6. This behaviour is due to the fact that the PMU needs to change the algorithm to adapt its performance to the different accuracy requirements of the M-class for different reporting rates.

The last two columns are related to the P configuration and are characterised by the lowest delay values. The results are similar for the two different reporting rates. This is because the electrical event is synchronised, and it is always located at the occurrence of second 10. The PMU sends its measurements at

Table 6. Evaluation of the latency of a PMU with different configuration.

Fs in fps	Input streams type	Max in ms	Mean in ms	St. Dev. in ms
10	P	39.3	38.9	0.1
	M	679.7	679.4	0.1
50	P	39.4	39.2	0.1
	M	135.82	133.3	0.1

Table 7. Evaluation of the latency in the protection test scenario for a PMU with different configuration.

Test	M class 10 fps in ms	M class 50 fps in ms	P-class 10 fps in ms	P-class 50 fps in ms
1	679.5	134.0	39.4	39.2
2	678.8	134.3	39.2	39.2
3	679.3	134.1	39.3	39.1
4	679.3	134.1	39.3	39.4
5	680.1	133.3	39.1	39.3
6	679.3	133.9	39.0	39.2
7	679.5	133.6	39.2	39.3
8	679.4	133.4	39.1	39.5
9	679.4	133.6	39.3	39.5
10	679.7	133.3	39.4	39.0

multiples of the nominal cycles second with respect to the UTC second and thus, in the considered test, the event instant and the timestamp of the corresponding measurement are equal. Indeed, it is possible to make the different contributions of delay explicit, as follows:

$$T_{delay} = T_l + T_p - \Delta T \qquad (1)$$

The overall delay T_{delay} of the event detection depends on the PMU reporting latency T_l and the processing time T_p of the PDC that is necessary for evaluating the data and for setting the digital output. The last term of the expression (ΔT) is the difference between the timestamp related to the first measurement, where the change of frequency is detected, and the time location of the electrical event. If the processing time T_p is low (as it is in the case at hand) and the event is located at the occurrence of the second, the overall delay is close to the PMU reporting latency and does not depend on the reporting rate. In this scenario, the PDC prototype, thanks to the continuous evaluation of the latency of the input streams, also provides a good evaluation of the delay.

A second test is then performed to emphasise the role of the event occurrence instant in the overall delay focusing on the P-class, since for this class, T_l is independent of Fs. In this scenario, the time position of the frequency step change is moved forward of 50 ms from $t = 10$ s to $10 = 10.05$ s. The detection of the event is located at different measurement instants, depending on the configured reporting rate. Table 8 reports the delay between the frequency step change and the digital output signals provided by the PDC prototype when the reporting rates are 10 or 50 fps. The P-class algorithm of the commercial PMU does not change its latency as shown in Table 6, but the overall delay depends on the chosen reporting intervals. Comparing the first and second columns, the impact of the reporting instants to the promptness of the system emerges. Furthermore, in this case, Equation (1) holds true, and the low delay contribution introduced by the

Table 8. Evaluation of the overall delay in the protection test scenario for a P-class PMU with different reporting rates.

Test	P10 fps in ms	P50 fp in ms
1	89.4	49.2
2	89.3	50.0
3	89.4	49.2
4	89.4	49.2
5	89.3	49.1
6	89.7	49.0
7	89.3	48.9
8	89.2	49.0
9	89.6	49.6
10	89.3	49.4

PDC is confirmed. As a practical rule, a fast response algorithm and high reporting rates are important prerequisites for minimising the overall delay of the protection system.

6. CONCLUSION

Synchrophasor technology is becoming an important tool for operators to monitor electric systems over a wide area in real time. Currently, this technology is viewed with interest not only for transmission grids, but also for distribution networks. In this context, with the aim of exploring the possibilities for synchrophasor-based monitoring architectures, this paper has presented a prototype of an active PDC developed with low-cost hardware. The feasibility of the proposal was evaluated in terms of the capability of the system to deal with time synchronisation at a good level of accuracy, thus also enabling nontrivial data management. The prototype is also able to safely manage several PMU data streams with different reporting rates and is thus promising as a building block for complex smart grid monitoring architectures. The PDC allows data latency estimation and is thus particularly useful for both real-time monitoring and control. The active PDC is equipped with a digital I/O interface and supports digital protection outputs with low additional delay. It can thus implement decision strategies based on input measurement data and latency evaluation.

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