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Research trends and challenges in testing digital-to-analog converters

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ABSTRACT
Today, a broad range of different applications relies on digital-to-analog converters. Different digital-to-analog converter architectures have been developed over the years, and several different specifications exist for quantifying their effective performance, the essential information to verify the requirement fulfilment, and the digital-to-analog converter's suitability for the specific application. As a result, testing digital-to-analog converters has assumed and continues to assume increasing importance. The main testing challenges include the reduction of the testing time and costs; the measurement uncertainty computation; and emerging built-in self-test solutions. To clarify digital-to-analog converter terms, definitions, and test methods, IEEE Standard 1658 has been developed and is currently undergoing revision. To highlight the trends and issues that provide useful information for the revision of the standard, this article presents an overview of the recent research work dealing with digital-to-analog converter testing.

Section: RESEARCH PAPER

Keywords: DAC; test; IEEE 1658 standard; non-linearity; uncertainty.

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1. INTRODUCTION

Digital-to-Analog Converters (DACs) perform an essential function in signal processing, since they allow circuits operating on digital signals to be connected with circuits operating on analog signals.

The number of applications relying on the DAC function is continuously increasing, including display electronics, motor control, software defined radio, data acquisition systems, optoelectronics, and test/measurement equipment.

DACs can also be components of larger circuits; for example, in successive-approximation Analog-to-Digital Converters (ADCs). On the other hand, advanced high-speed DACs can embed digital signal processing and conditioning functionalities, such as complex modulation; digital filters and interpolators; and numerically controlled oscillators [1].

New DAC architectures and techniques continue to be developed in order to meet specific application requirements, demanding higher and higher DAC performance and assessing it more stringently. Therefore, DAC specification comparison and assessment are complicated by the variety of requirements, underlying conditions, and DAC architectures.

To bring order and clarity to the field in DAC terms and definitions as well as to provide proper DAC test methods, IEEE Standard 1658 has been published in 2012 [2], and it is currently under revision. Previous work has been developed in the past on DAC testing research directions [3]. However, in recent years, DAC architectures and application contexts have continuously and rapidly evolved. Consequently, new challenges and points of interest have arisen, leading to the need for an update to IEEE Standard 1658, as well.

To provide useful information on the standard's update process, a brief review of the latest research on DAC testing has been presented in [4].

This study is an extended version of [4], which aims to highlight the prevailing issues and needs in the field that should be considered in the revision of IEEE Standard 1658. In the first section, the DAC research trends are briefly introduced. Then, focus is given to some recent research contributions, organised in four subsections, dealing with DAC static and dynamic testing;

figures of merit; and measurement uncertainty. Finally, conclusions are drawn.

2. DAC RESEARCH TRENDS

Much of the scientific literature addressed to data converters continues to be devoted to ADCs. An overview of the gap that exists between the number of ADC and DAC research contributions is given in [5]: 'ADC papers in the circuits' conferences often outnumber the DAC papers by 3:1 or more'.

Concerning DAC research, recent contributions have mainly focused on architecture design topics for optimising performance according to different application requirements. Many design strategies have been developed for dealing with DAC error sources [6], like DAC modelling [7]-[9] and calibration methods [10]-[12]. There are fewer scientific works that instead focus on testing DACs.

The topics addressed by the researchers in this field concerning DAC static testing are mainly devoted to the reduction of the test time and costs, also by means of the development of efficient DAC Built-In Self-Test (BIST) solutions operating in System-on-Chip (SoC) and System-in-Package (SiP) environments. Regarding, instead, the DAC dynamic testing, research has focused on overcoming the difficulties experienced in the characterisation of some specific DAC parameters.

Hand in hand with DAC technological development, research interests have been directed towards DAC figures of merit in order to analyse and overcome the limitations of the conventional ones; to propose new ones that better reflect the needs of the specific applications; and to define the requirements for the figure of merit of interest depending on the specific application or reference standard.

Finally, even more research work has focused on the lack of measurement uncertainty estimation procedures.

In the following subsections, some research contributions belonging to the abovementioned DAC testing topics are briefly presented.

2.1. DAC static testing

DAC static testing is aimed at characterising the converter response to DC or low-frequency input signals. Typical DAC static specifications are the gain, offset, Integral Non-Linearity (INL), and Differential Non-Linearity (DNL).

With the increasing demand for high-performing DACs along with increasing resolutions, the required DAC testing time increases exponentially, hand in hand with the test cost. This is especially true in the case of DAC static linearity testing, since it traditionally requires a long time and is very expensive.

The testing method and algorithm introduced in [13] form a solution for accurate DAC linearity testing with reduced test time and costs. The proposed algorithm comes from the consideration that the number of independent error sources is, in most cases, much smaller than the number of DAC codes examined in the linearity test. Therefore, it is possible to carry out linearity testing with much fewer samples, which saves the test time. In particular, the number of unknowns that must be evaluated is decreased in [13] by means of a segmented non-parametric model for the INL curve of the DAC.

Moreover, the proposed method involves the use of an on-board digitiser for DAC output measurement in place of a highly accurate digital voltmeter, resulting in less test time per sample. This test time reduction has the direct consequence of reducing the test costs, too. Additionally, the measurement error introduced due to the on-board digitiser is removed in the proposed algorithm, relaxing the stringent linearity requirement on the measurement device, allowing it to be orders of magnitude less linear than the DAC under test, implying further cost savings. The proposed method can be applied to DAC architectures inherently segmented, as binary weighted, R-2R and mDAC, but it is not valid for string or thermometer-coded architectures [13].

Other proposals for overcoming the requirements for high performance testing equipment and for avoiding the direct transfer of analog signals to external instruments are based on BIST approaches.

One example is the low-speed BIST scheme for testing DAC static parameters presented in [14]. The proposed approach is based on an under-sampling technique. The DAC analog signal is modulated by the two sinusoidal carriers and then converted into a low-speed pulse stream. The relationship between the non-linearity of the DAC and the width of pulse stream can be further derived. Moreover, the required operational frequency of the testing equipment used in the proposed scheme is much lower than that of DAC [14]. In Figure 1, the scheme for the proposed method along with the signals involved are shown. In particular, the BIST approach relies on the use of a sinusoidal carrier generator, two comparators, a logic control unit, a Time-to-Digital Converter (TDC), and an all-pass filter acting as a delay element. The all-pass filter provides the sinusoidal carrier with a phase delay t_d [Figure 1 (b)]. The comparators modulate the DAC

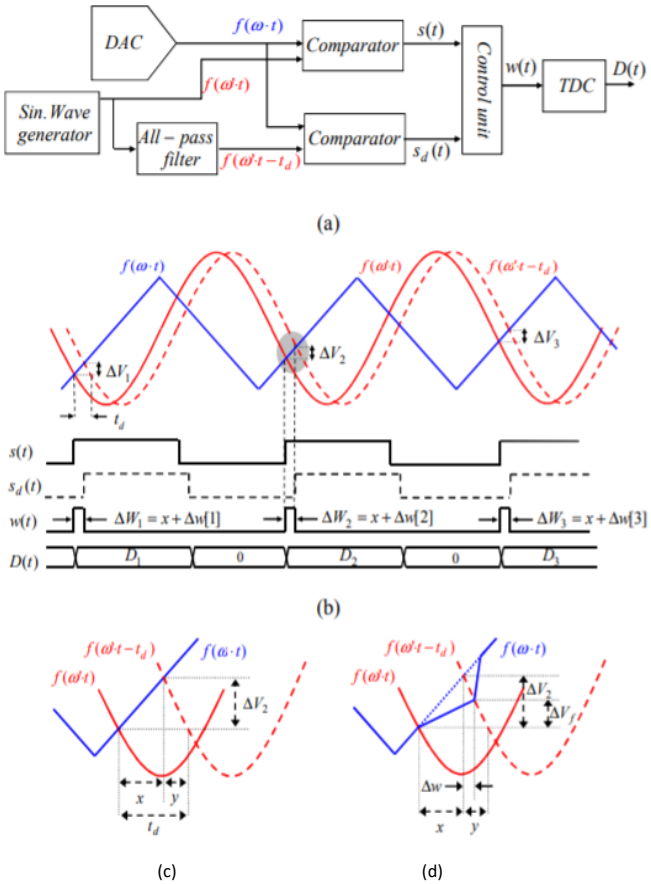

Figure 1. (a) The scheme of the proposed method with the dual undersampling technique. (b) The relative signals. (c) The shadow area in Figure 1 (b) of the linear case. (d) The shadow area in Figure 1 (b) of the non-linear case [14].

output signal by both carriers, resulting in a narrow phase difference between two digital streams that represent the non-linearity variation of the DAC output signal. The logic unit provides the phase difference of the two digital streams, and the TDC converts these pulse widths into readable binary codes. In Figure 1 (c) and Figure 1 (d), the shadow area of Figure 1 (b) is enlarged to show the linear and the non-linear cases, respectively. Thanks to the very short duration between adjacent sample points, the sinusoidal carrier can be treated as the combination of piece-wise linear segments. As shown in Figure 1 (d), in the presence of non-linearities, the displacement of the cross point of the carrier and DAC output signal appears on the phase difference Δw. The method was validated on an 8-bit 200MS/s DAC, and it could be interesting to investigate the results obtained on DACs with greater resolution and speed.

The BIST structure for data converter static testing proposed in [15] focuses on the common case in which an ADC and DAC pair is embedded in a SoC. By testing both the ADC and DAC converters simultaneously, the resulting test time can be decreased compared to other BIST approaches (i.e. the loopback test). Moreover, the hardware overhead is reduced compared to that of the standalone BIST by sharing additional BIST circuitry for testing the converters. In Figure 2, the proposed BIST scheme is shown. A counter is used for transition detection in ADC testing and as a test pattern generator in DAC testing. The ramp generator is used as a test input generator for ADC testing and as a voltage reference for DAC testing. For simultaneous ADC and DAC testing, the timing for each test must be arranged in order to share the use of the counter and the ramp generator. The proposed method is applicable to ADC and DAC with the same 1 LSB length and with the same or a different resolution. In this last case, the sampling frequencies of the two converters must be chosen to have the same time ticks [15].

2.2. DAC dynamic testing

DAC dynamic testing is aimed at characterising the converter response as the frequency and amplitude of the input signal's variance. Specifications describing the DAC dynamic performance include the settling time, glitch, Spurious-Free Dynamic Range (SFDR), Total Harmonic Distortion (THD), Signal-to-Noise Ratio (SNR), Signal-to-Noise-and-Distortion Ratio (SINAD), Effective Number of Bits (ENOB).

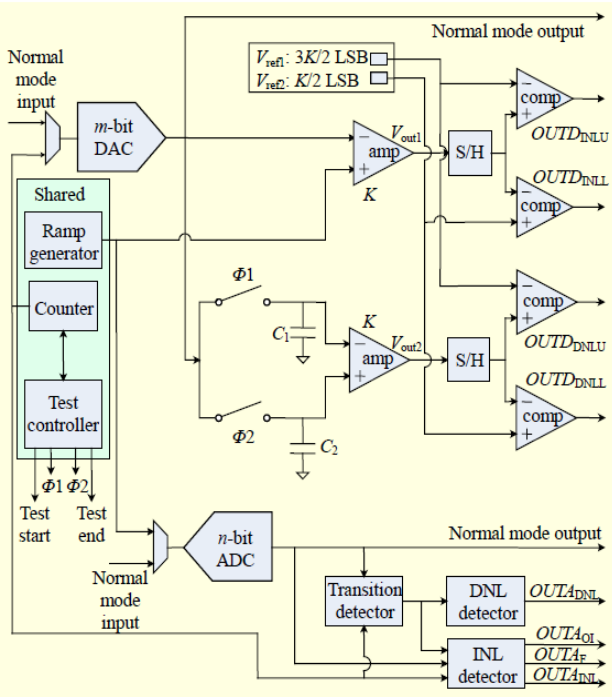

Figure 2. The BIST scheme proposed in [15].

DACs are currently used in a wide number of different applications, each with its own sensitivities to different dynamic specifications. Consequently, research work on DAC testing can be focused on a particular specification of interest.

The settling time of the output signal is one of the most important parameters characterising high-speed DACs. However, it is also challenging to test the parameter accurately.

A method that aims to automatically measure the settling time of high-speed DACs with a mid-high resolution has been proposed and experimentally investigated in [16]-[18]. In particular, in order to perform the automatic measurement of the settling times of 12-bit DACs (or more), the DAC output signal is converted to digital form, and digital signal processing is performed [16][17].

The algorithms proposed in [16][17] show the possibility of measuring the settling time of the high-speed DACs with up to 16-bit resolution [18]. Moreover, by using those algorithms, it is possible to reduce the level of 1/f and white noise by 100 times without distorting the measurement signal itself.

Another relevant specification for high-speed and high-accuracy DACs is represented by glitches. The DAC glitches can actually compromise the overall converter spectral performance, making it unsuitable for specific applications. Unfortunately, different definitions and testing methods exist, making misinterpretations of the real DAC performance possible.

An experimental analysis of the different DAC glitch definitions and measurement methods proposed in the literature and adopted by manufacturers is provided in [19]. In particular, experimental investigation into the reproducibility of the results that can be achieved on the DAC by varying the definitions and the testing methods has focused on (i) the applicability of each glitch definition and testing method; (ii) the required computational complexity; and (iii) the possibility of automating the area measurement procedure, excluding the need for operator supervision. Preliminary results have shown that the restriction of the oscilloscope bandwidth greatly influences the estimation of the glitch values. An analysis of the numerical integration methods that can be applied to compute the glitch has been focused on the rectangle methods (the right and left corner; maximum and minimum corner; and the midpoint), the trapezoid, and Simpson's methods, as shown in Figure 3. This analysis has also highlighted in this case the influence of noise on the results. Moreover, the number of samples considered for the numerical integration greatly affects the confidence of results, representing a critical problem since in the case of very small and fast glitches, only a few samples can be captured. Further research work is needed for comparing different definitions and testing procedures for DAC glitches by analysing different converters. In addition, the glitch waveform dependence from the used measurement equipment should be investigated [19].

2.3. DAC Figures of Merit

DAC technological developments have led the research to focus on the DAC figures of merit in order to introduce new ones that are capable of overcoming the conventional figures of merit limitations as well as to find their relationships with other relevant parameters, or specific requirements for the particular application or reference standard.

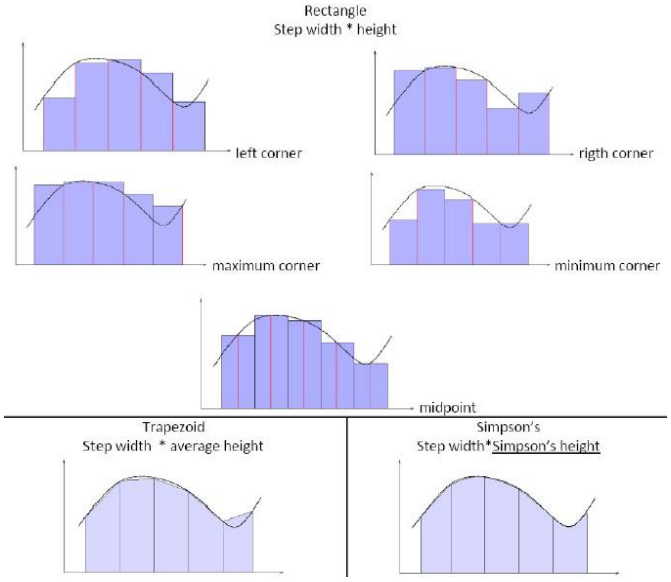

Figure 3. The numerical integration methods analysed in [19].

DAC performance is typically described by using figures of merit, focusing on the expected overall linear behaviour [20].

However, considering the internal structure and the electronic components embedded in the DAC can provide a more reliable description of the system as well as a better explanation of the nature of the deviations observed at the DAC output [20].

To achieve this target, a DAC system model and a new figure of merit are presented in [20]. In particular, the proposed model consists of two blocks: The first includes a set of individual current (voltages) sources followed by a switching array, the second represents a summation step. The proposed DAC model has been carried out in order to incorporate deviations at sources and switches as well the quantisation noise in the first block and deviations, which refer to the summation circuit in the second block [20]. A non-linearity assessment procedure is then introduced based on a generalised Hammerstein network, including a prominent linear term associated with the input, additive, order-dependent, distortion terms, and an additive filtered noise term [20]. In this way, DAC performance can be carried out by separately taking into account both the deviations at the input sources and switches as well as the nonidealities in the posterior summation circuit, allowing for the analysis of the cross influence between these two effects, too [20].

The novel figure of merit, named the system residue, is introduced in [20] to describe the full-scale DAC response along the full input frequency span. This new DAC parameter is able to separate the contributions of the different blocks in the system, such as the DAC's inner structure nonlinear deviations and memory effects, in such a way that it is easy to interpret by simple inspection [20].

In wideband communication systems, the half-rate interleaved topology is often employed in Nyquist current-steering DACs in order to obtain an ultra-high sampling rate. For this kind of DAC, the duty cycle error is a main contributor to performance degradation [21]. However, little research has focused on this parameter [21].

To investigate the duty cycle distortion under the influence of limited output bandwidth in interleaved Nyquist DACs, a closed-form expression of the parameter's Signal-to-Distortion Ratio (SDR) based on the Heaviside function is introduced in [21]. In particular, the SDR has two components, the former intrinsically caused by duty cycle error and the latter by limited bandwidth. In order to verify the SDR's mathematical derivation, some simulations have been carried out in [21] by means of a model of a 6-bit 25GS/s DAC (based on the half-rate architecture), with a 50 Ω terminal load. The simulation results are discussed within the 1st-Nyquist band, and the limited bandwidth is determined by the output time constant τ, depending on the output parasitic capacitance [21]. In Figure 4, the simulated and calculated SDR changes with duty cycle error, varying from 0 to 10 %, are shown with the different normalised input signal frequencies (f_{in}) in mind, from low to the 1st-Nyquist bandwidth and a fixed value for the output time constant. It is evident the great influence of the duty cycle error on the dynamic performance, proven by the SDR degradation (>10dB), which corresponds to a 1 % duty-cycle error [21].

The distortion caused by the duty cycle has been shown to worsen as the input frequency rises, and the worst case is near the Nyquist input frequency due to the impact of the limited bandwidth. SDR can therefore be used to evaluate the performance of interleaved half-rate DACs [21].

DAC phase noise is a crucial parameter for all the systems that require high-purity RF signals [22][23]; for example, in radar applications [24]. However, from the analysis of numerous DAC datasheets, it can be derived that the phase noise as well as amplitude noise performance have been poorly documented [22][23]. Therefore, a method of measuring both the DAC amplitude and phase noise by means of a phase noise analyser was proposed in [22][23]. The proposed method is described to have the advantage of requiring relaxed noise specifications for the phase noise analyser, by a factor of at least 20 dB, with respect to the noise of the device under test. This can be obtained thanks to the RF amplification of the noise sidebands and the possibility of measuring the amplitude noise through a phase noise analyser, not including this measurement feature. The same measurements can be performed by using only an amplitude noise analyser (i.e. a power-detector diode followed by a FFT analyser), without the phase noise measurement capability [22][23].

In addition to the phase noise in the frequency domain, the focus of this research is also on its relative in the time domain, the jitter [25]-[30]. Research works have included the modelling of its effects for particular DAC architectures [25][26] and the definition of the parameter requirements and the impacts thereof in specific applications [29][30].

2.4. Measurement uncertainty

Currently, evaluation of the measurement uncertainty has not yet been included in any DAC standard. The measurement

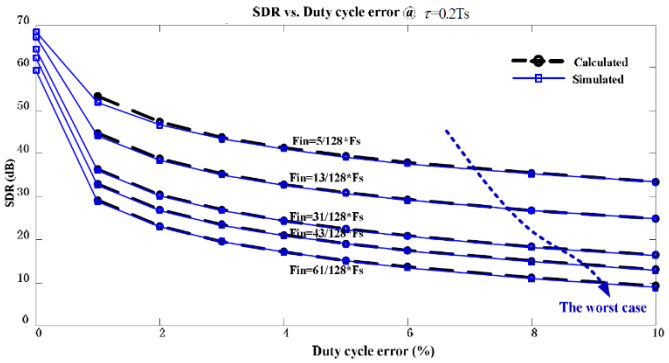

Figure 4. Simulated and calculated SDR changes with the duty cycle error at output time constant τ = 0.2Ts [21].

uncertainty is a quantitative indication of the quality of the measurement and is essential for comparing results coming from different sources or with reference values given in specifications or standards. Although ADC research works dealing with the measurement uncertainty have been developed [31]-[35], the same was not found for DACs. Very few papers have been published in this field.

An example can be found in [36]: An evaluation of the measurement uncertainty of time domain dynamic parameters, as the DAC rise time and fall time relying on a bootstrap technique according to the 'Guide to the expression of uncertainty in measurement' [37] was presented. The proposed approach allows us to define confidence intervals from short acquisition records without needing hypotheses about the measurand distribution, in an easy and fast way, to ensure that the method can be also applicable in an industrial environment. However, since the approach deals only with the rise time and fall time, it would be useful to extend its application to other DAC parameters.

A new DAC testing method together with its analysis from the uncertainty point of view is provided in [38][39]. The test is based on the comparison of a time-varying saw-tooth signal generated by the converter under test with a reference signal by a fast comparator. The reference signal is the superposition of the DC voltage measured by a precise DC voltmeter and slow dithering voltage with a known amplitude. The comparator detects the sequence of the DAC control codes, which determine the DAC nonlinearities. The proposed method has been validated both by simulations and experiments in a real setup under different working conditions. In Figure 5, the simulation of the combined dependence of the uncertainty on record length (considering different numbers of samples L as well as on the amplitude of dithering W) is shown. Simulation results show that by increasing amplitude W, the uncertainty grows approximately linearly, with the record length with the highest impact on the final uncertainty [38][39]. In particular, by increasing the number of samples, the uncertainty can be decreased, but at the cost of a longer measuring time. Consequently, a compromise between the required uncertainties and the acceptable measuring time depending on user needs has to be made [39].

3. CONCLUSIONS

Today, an extremely large and growing number of new and rapidly evolving applications rely on DAC functionality and performance. Data converter design and testing are strictly related to the stringent performance specifications required by their reference application, also continuing to keep pace with technological advances.

In the article, a brief overview of the latest research on DAC testing has been presented in order to provide worthwhile information for the revision of the IEEE standard dealing with the terminology and test methods of DACs.

Most of the relevant research has focused on DAC architecture design strategies aimed at achieving the best performance in the specific application context. Even fewer research contributions can be found concerning DAC testing.

Recent research in this particular field has mainly aimed at providing mostly static testing methods requiring reduced time and cost, also paying attention to the situation in which the DAC operates in a SoC or in an SiP. Another source of the research interest is the testing of some specific dynamic parameters, like settling time and glitch, due to the challenging measurement

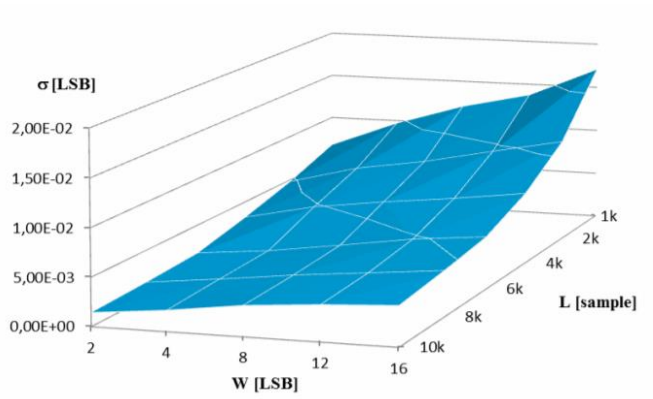

Figure 5. Dependence of the standard deviation of difference between the INL characteristics on the amplitude of dithering W and different numbers of samples L [39].

maintaining suitable accuracy of the first one for high-speed DACs as well as the ambiguity in the developed definition and testing methods of the second one.

New DAC figures of merit capable of answering to some specific needs of the target applications are also objects of the relevant research. The opportunity of changing the conventional DAC figures of merit and the definitions of their requirements to comply with the existing reference standards or emerging application needs have also sparked this research interest.

Unfortunately, measurement uncertainty evaluation has turned out to be an overlooked argument for DAC testing. However, information about this parameter is essential in the evaluation of the effectiveness of the proposed DAC testing methods and in comparing DAC specifications. There is still a great deal of research to do on this specific aspect.

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