Soft-Charging Effects on a High Gain DC-to-DC Step-up Converter with PSC Voltage Multipliers

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Abstract−**This paper proposes a split-phase control diagram for a new design of a DC-to-DC boost converter which is called PSC-boost and studies its performance. The PSC-boost has two sides, the primary is a PSC converter and the secondary is a DC-to-DC boost converter. The effect of applying the split-phase control diagram helps reduce the output impedance successfully and increases efficiency by 3%. The simulated and analytical results have been proven to validate the effect of the split-phase diagram. The simulated design contains five switches, five capacitors, seven diodes, and three inductors to step up 10V into 160V at 200KHz and 100KHz switching frequencies. The LTspice simulator was used to design and test the proposed model.**

Keywords-PSC-boost converter; split-phase diagram; SC converters; LTspice

I. INTRODUCTION

Renewable energy has been proven to be an essential sustenance of conventional energy resources. Sustainability and eco-friendliness are two motivations that motivate hundreds of renewable energy research projects, but the low produced power limits its usage, for instance, PV cells produce a voltage that ranges between 12 to 48V. To overcome this limit and expand renewable energy applications, boosting the DC produced voltage to a higher voltage level by using DC-to-DC boost converters is recommended. Furthermore, DC-to-DC converters help finding the appropriate integration between renewable energy sources and grid utilities. There are two types of DC-to-DC boost converters: isolated or non-isolated converters. Their main difference is that the isolated design has a power transformer that divides the converter into primary and secondary sides. Having a power transformer increases the voltage gain, however it can produce electromagnetic interference. Lower power density is another side effect of using a power transformer. Thus, a non-isolated conventional boost converter is preferable over the isolated DC-to-DC converter due to the absence of the power transformer. Duty cycle dependency and voltage inductor second balance are two operational aspects of the non-isolated boost converter. The proportional relation between the duty cycle and high voltage gain makes the increase in the duty cycle the only way to provide a higher voltage gain. However, the increase of duty cycle is limited by switches' voltage stress, which could harm the converter's efficiency. There are several alternative ways to increase the voltage gain at a lower duty cycle, such as adding voltage multipliers to the DC-to-DC boost converter [1, 2]. Besides that, using a resonant approach for DC-to-DC converters, shows great improvement of the converters efficiency [3, 4]. The new DC-to-DC converter is known as a Multilevel Boost Converter (MBC). Adding more output multipliers and keeping the main converter part (primary side) is the main aspect of the MBC converter [5-13]. The MBC increases the regulated output voltage by adding voltage cells, which are basically switched capacitors cells, but have drawbacks, such as the failure to produce the actual output voltage at higher duty cycles [14]. The proposed model in [14] uses a switched capacitor converter (PSC) as a primary stage on a conventional boost converter. The switched capacitors cells work similarly with the MBC converter, however, they are connected to the primary side of the conventional boost converter. The PSC-boost converter has shown superiority in the efficiency and actual rated voltage achievement in comparison with the MBC converter. In [15], the proposed control diagram helps achieving the complete soft-charging operation. The proposed split-phase diagram helps in increasing the efficiency by reducing the PSC converter's output impedance.

This paper complements our work in [14] by using a split-phase control diagram [15] to operate the 8 switches of the PSC-boost. The implemented control diagram increases effectively the PSC-boost efficiency in reducing the output impedance. Analytical and simulated results are presented.

II. THE PSC SWITCHED-CAPACITOR CONVERTER

A. Topology and Operation

Figure 1 shows the topology of the 1-to-4 PSC converter and its control signals. The control diagram in Figure 2(a) shows how four modes of operation are possible. In each mode, the capacitors are connected to each other differently for voltage regulation purposes. In Mode-1, the flying capacitor C_{f1} is charging and the flying capacitor C_{f2} is discharging. In Mode-2, both flying capacitors C_{f1} and C_{f2} are discharging and in Mode-4 they are both charging. In Mode-3 C_{f1} is discharging and C_{f2} is charging. To find the gain voltage of the proposed converter, each mode has a total charge that can be derived from the following equations [15-18]:

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$$QT_i = V_{C_1}C_1 + V_{C_2}C_2 + V_{C_{f1}}C_{f1} + V_{f2}C_{f2} \quad (1)$$

where i is the number of modes (1, 2, 3, 4). From Mode-1 (Figure 2) we have:

$$V_{C_{f1}} = V_{C_1} \quad (2)$$

$$V_{C_2} = V_{C_{f2}} \quad (3)$$

$$V_{C_{f1}} = V_o - V_{in} - V_{C_{f2}} \quad (4)$$

B.y substituting (2), (3) and (4) in (1) we get the total charge of Mode-1 (5):

$$QT_1 = V_{in}(-C_{f1} - C_1) + V_{f2}(C_2 + C_{f2} - C_1 - C_{f1}) + V_o(C_1 + C_{f1}) \quad (5)$$

To find the total charge of the rest of the modes, the same steps can be repeated:

$$QT_2 = V_{in}(C_{f1} - C_1) + V_{f2}(C_1 + C_{f2} - C_2) + V_{out}C_2 \quad (6)$$

$$QT_3 = V_{in}(-C_{f1} - C_1) + V_{f2}(C_1 + C_{f1} + C_{f2} - C_2) + V_{out}C_2 \quad (7)$$

$$QT_4 = V_{in}(C_{f1} - C_1) + V_{f2}(-C_1 + C_{f2} + C_2) + V_{out}C_1 \quad (8)$$

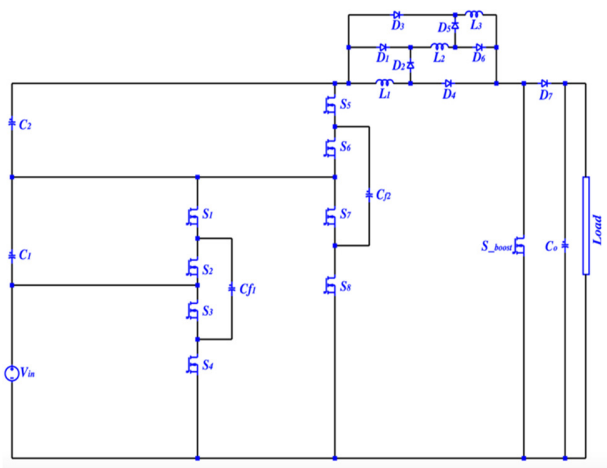

Fig. 1. The 2-level of the proposed PSC-boost converter.

In the steady state operation, the total charge of any pair of modes is assumed to be equal. In this work, we assumed that:

$$QT_1 = QT_4 \quad (9)$$

$$QT_2 = QT_3 \quad (10)$$

By simplifying (9) and (10) we get:

$$2V_{in}C_{f1} + V_{f2}C_{f1} - V_{out}C_{f1} = 0 \quad (11)$$

$$2V_{in}C_{f1} - V_{f2}C_{f1} = 0 \quad (12)$$

By combining (11) and (12), the 1-to-4 PSC converter's voltage gain can be calculated (13):

$$V_{out} = 4V_{in} \quad (13)$$

The general form of the proposed converter is:

$$V_{out} = 2^n V_{in} \quad (14)$$

where n is the number of the stage.

B. Slow-Switching Limit Impedance (R_{ssl})

The SC converters suffer from losses related to the switches' switching and the capacitors' charging or discharging process. This capacitors' loss can be characterized as an output impedance that is called a slow switching limit impedance R_{ssl}. The charge flow analysis of the four modes has been applied to find the charge multiplier of the four capacitors a_c^i

$$q_c^i = a_c^i\, q_{out} \quad (15)$$

$$q_c = [q_{C_1} q_{C_2} q_{C_{f1}} q_{C_{f2}}]^T \quad (16)$$

In [13, 14] a useful technique was used to find the charge flow's vector of all the operation modes. For the ith mode, KCL can be derived by:

$$B_i q^i = 0 \quad (17)$$

where B_i represent the reduced incidence matrices of the four modes of 1-to-4 PSC converter:

$$B_1 = \begin{bmatrix} -1 & -1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & -1 & -1 & 0 \\ 0 & 0 & -1 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \quad B_{2,a} = \begin{bmatrix} -1 & -1 & 0 & -1 & 0 & 0 \\ 0 & 1 & 1 & 0 & -1 & 0 \\ 0 & 0 & -1 & 0 & 0 & -1 \\ 1 & 0 & 0 & 1 & 1 & 1 \end{bmatrix}$$
$$B_{3,a} = \begin{bmatrix} -1 & 1 & 0 & -1 & 0 & 0 \\ 0 & -1 & -1 & 1 & -1 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \quad B_{4,a} = \begin{bmatrix} -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & -1 & -1 & 0 & -1 & 0 \\ 0 & 0 & 1 & 0 & 1 & -1 \\ 1 & 0 & 0 & -1 & 0 & 1 \end{bmatrix} \quad (18)$$

To find the charge flow's vectors, (17) can be solved for q^i:

$$q_{Flow}^1 = \begin{bmatrix} -3 \\ 1 \\ -1 \\ -2 \\ 2 \\ 3 \end{bmatrix} \quad q_{Flow}^2 = \begin{bmatrix} -3 \\ 1 \\ -3 \\ 2 \\ -2 \\ 3 \end{bmatrix} \quad q_{Flow}^3 = \begin{bmatrix} -2 \\ -1 \\ 3 \\ 1 \\ -1 \\ 3 \end{bmatrix} \quad q_{Flow}^4 = \begin{bmatrix} -2 \\ -3 \\ 2 \\ 1 \\ 1 \\ 3 \end{bmatrix} \quad (19)$$

The total output charge with respect to the output charge can be found in (20):

$$q_{out} = q_{out}^1 + q_{out}^2 + q_{out}^3 + q_{out}^4 \quad (20)$$

The total output charge with respect to the input charge is:

$$q_{out} = q_{in} + q_{in} + \frac{3q_{in}}{2} + \frac{3q_{in}}{2} = 5q_{in} \quad (21)$$

By using (21), (19) can be rewritten with respect to the output charge (22):

$$q_c^1 = \begin{bmatrix} \frac{q_{out}}{5} \\ \frac{-q_{out}}{5} \\ \frac{-2q_{out}}{5} \\ \frac{2q_{out}}{5} \end{bmatrix} \quad q_c^2 = \begin{bmatrix} \frac{q_{out}}{5} \\ \frac{-3q_{out}}{5} \\ \frac{2q_{out}}{5} \\ \frac{-q_{out}}{5} \end{bmatrix} \quad q_c^3 = \begin{bmatrix} \frac{-q_{out}}{5} \\ \frac{3q_{out}}{5} \\ \frac{q_{out}}{5} \\ \frac{-q_{out}}{5} \end{bmatrix} \quad q_c^4 = \begin{bmatrix} \frac{-3q_{out}}{5} \\ \frac{2q_{out}}{5} \\ \frac{q_{out}}{5} \\ \frac{q_{out}}{5} \end{bmatrix} \quad (22)$$

By applying (15), the charge multipliers are:

$$a_c^1 = \begin{bmatrix} \frac{1}{5} \\ \frac{-1}{5} \\ \frac{-2}{5} \\ \frac{2}{5} \end{bmatrix} \quad a_c^2 = \begin{bmatrix} \frac{1}{5} \\ \frac{-3}{5} \\ \frac{2}{5} \\ \frac{-1}{5} \end{bmatrix} \quad a_c^3 = \begin{bmatrix} \frac{-1}{5} \\ \frac{3}{5} \\ \frac{1}{5} \\ \frac{-1}{5} \end{bmatrix} \quad a_c^4 = \begin{bmatrix} \frac{-3}{5} \\ \frac{2}{5} \\ \frac{1}{5} \\ \frac{1}{5} \end{bmatrix} \quad (23)$$

Then by using Tellegen's theorem, R_{ssl} can be found for the proposed design:

$$\frac{V_{out}}{q_{out}} + \sum_{i=1}^{number\ of\ C} \frac{(a_{c,i})^2}{C_i} = 0 \quad (24)$$

where $\frac{V_{out}}{q_{out}} = R_{ssl}$.

$$R_{ssl} = \sum_{i=1}^{number\ of\ C} \frac{(a_{c,i})^2}{C_i} \quad (25)$$

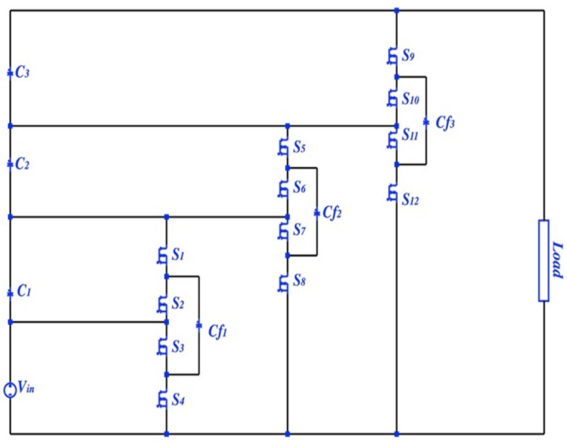

Fig. 2. 1-to-8 PSC topology (three-stage).

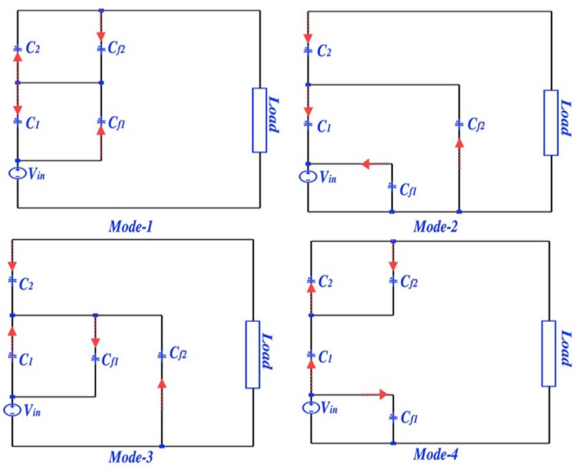

Fig. 3. The charge flow direction for each operation mode.

C. Fast-Switching Limit Impedance

Another important parameter in the SC converters' analysis is finding the fast switching limit (R_{Fsl}). In the SC converter two parameters are responsible for increasing efficiency, which are high switching frequency and large capacitor size. The R_{Fsl} depends on the switches' R_{ds_on} as:

$$R_{Fsl} = \sum_{i=1}^{number\ of\ S} (a_{r,i})^2 \quad (26)$$

where $(a_{r,i})$ is the charge multiplier of eight switches in the 1-to-4 PSC converter.

III. A COMPARISON BETWEEN THE PROPOSED PSC CONVERTER WITH THREE SC CONVERTER TOPOLOGIES

The comparison between the proposed PSC and three known SC converter topologies (1-to-4 series to parallel, 1-to-4 ladder, and 1-to-4 Dickson) considers the fundamental efficiency and the output impedance. The PSC converter is found to be superior over the three other topologies in high efficiency achievement whereas the 1-to-4 ladder has the lowest efficiency (Figure 4). In addition, the PSC converter successfully achieves the SSL limit at a lower switching frequency faster than the other topologies (Figure 5). In other words, the PSC converter requires less switching frequency to achieve lower output impedance. The second lowest output impedance among the compared topologies is accomplished by the series to parallel topology, which means that an additional comparison must be calculated between the PSC converter and 1-to-4 series to parallel considering the number of switches and the maximum voltage stress across the switches [19-24].

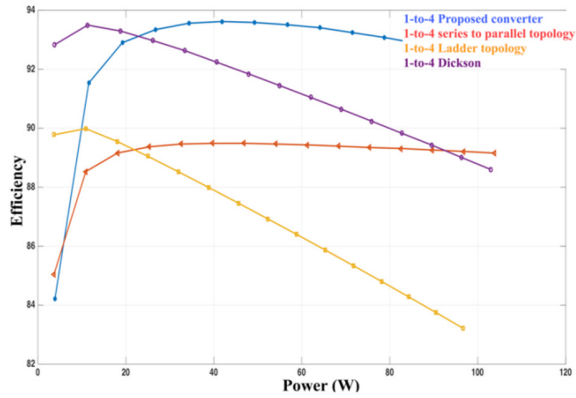

Fig. 4. Efficiency vs rated power.

IV. THE PROPOSED MODEL

The PSC switched-capacitor converter can be used as a voltage multiplier and as a primary stage of a non-isolated boost converter. The multiplier cells can be increased with regard to the desired output voltage without distorting the conventional boost converter side. Capacitors' charging and discharging processes are successfully demonstrated by fully controllable semiconductor devices, which are switches. The 8 switches are controlled by the proposed split-phase diagram that allows dead time for each switch. In addition to applying a split-phase control diagram, the proposed switched inductor cell in [25] is used as an input inductor in the boost converter side (second-stage). The proposed control diagram is based on the increase of the periods of the transitions modes which are between any two existing modes. This allows a dead time for all eight switches (Figure 3). Applying the split phase control diagram helps to reduce the output impedance, thus exhibiting the converter's efficiency. Adding more modes would reduce the charge multipliers of each capacitor and thus reduce the

output impedance. To reduce the output impedance by using the convectional control diagram requires a higher switching frequency. This requirement can be recovered by applying the split-phase control diagram where the output impedance can be maintained low at a lower switching frequency. Table I exhibits the comparison between the PSC output impedance for traditional and split-phase control diagrams.

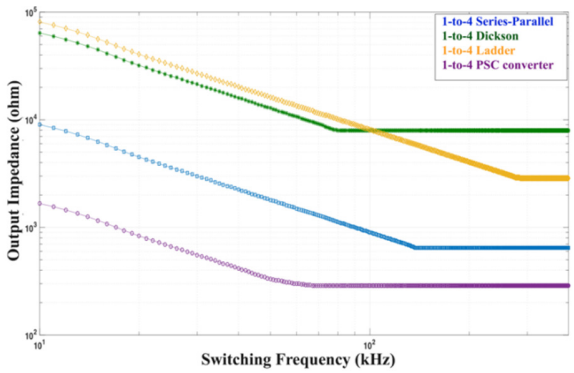

Fig. 5. Output impedance vs switching frequency.

TABLE I. COMPARISON BETWEEN THE PSC OUTPUT IMPEDANCE FOR TRADITIONAL AND SPLIT-PHACE CONTRO

Charging operation	R_{ssl}	$(a_{c,i})^2$
Conventional control diagram	$\frac{1}{6}\sum_{i=1}^{number\ of\ C}\frac{(a_{c,i})^2}{C_i\ fsw}$	$\frac{5}{2}$
Split-phase control diagram	$\frac{3}{20}\sum_{i=1}^{number\ of\ C}\frac{(a_{c,i})^2}{C_i\ fsw}$	$\frac{5}{18}$

V. ANALYSIS OF THE PROPOSED MODEL

The proposed converter has two stages, PSC converter and conventional boost converter (Figure 7). The boost stage has an input which is basically the PSC converter output voltage. When replacing the input inductor of the boost converter by the switched-inductor model which has three inductors L_1, L_2 and L_3, these three inductors are assumed to be ideal and equal. During Mode-1 to Mode-4, each of the three inductors has a voltage drop equal to V_{in} (27) due to their parallel connection:

$$V_{in} = V_{L1} = V_{L2} = V_{L3} \quad (27)$$

$$I_c = \frac{-V_{out}}{R_L} \quad (28)$$

where V_{out} and R_L are the output voltage and the load respectively. When S-boost is off, a series connection of L_1, L_2 and L_3 is exhibiting through Mode-5 to Mode-8:

$$V_{in} = V_{L1} + V_{L2} + V_{L3} + V_{out} \quad (29)$$

since L_1, L_2 and L_3 are the same, they will have the same voltage drop.

$$V_{in} = V_{L1} + V_{L2} + V_{L3} + V_{out} \quad (30)$$

$$3V_L = V_{L1} + V_{L2} + V_{L3} \quad (31)$$

We can rewrite (30) into (31) to get (32):

$$V_{in} = 3V_L + V_{out} \quad (32)$$

$$V_L = \frac{V_{in} - V_{out}}{3} \quad (33)$$

By assuming the inductor voltage's second balance to (27) and (33), the voltage gain of the proposed model can be obtained:

$$DV_{in} = -(1-D)\left(\frac{V_{in} - V_{out}}{3}\right) \quad (34)$$

The converter gain of the second stage can be found by:

$$\frac{V_{out}}{V_{in}} = \frac{2D+1}{1-D} \quad (35)$$

By substituting V_{in} in (35) by the output voltage of PSC we get:

$$\frac{V_{out}}{V_{out\_PSC}} = \frac{2D+1}{1-D} \quad (36)$$

$$V_{out\_PSC} = 2^N V_{in} \quad (37)$$

where N is the number of the converter stages.

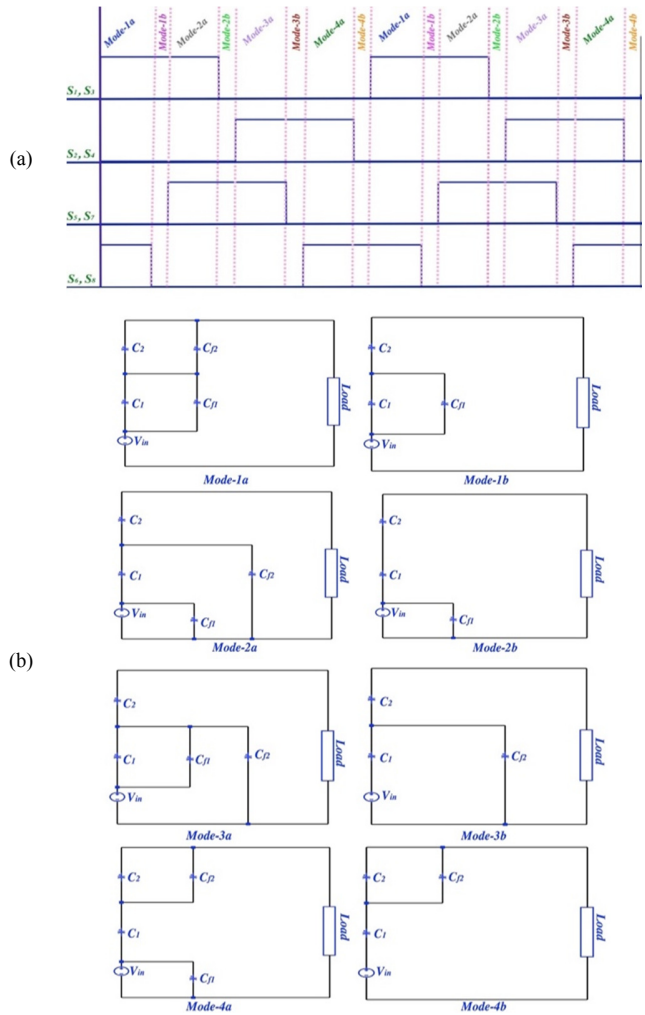

Fig. 6. (a) A proposed timing diagram for the split-phase operation for the 1-to-4 PSC converter, (b) The 8 operation modes of the 1-to-4 PSC converter after applying the split-phase.

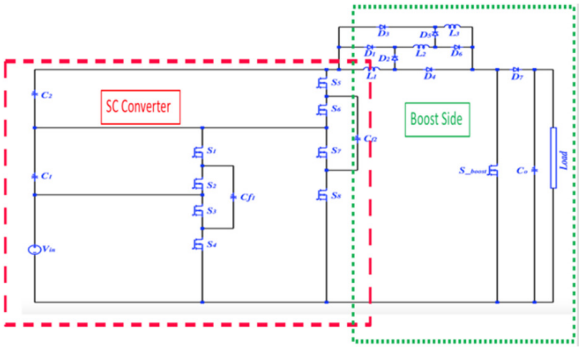

Fig. 7. The proposed converter and its two stages, PSC converter and conventional boost converter.

By rewriting (36), the voltage gain of the PSC-boost converter can be represented as:

$$\frac{V_{out}}{V_{in}} = \frac{2^N(2D+1)}{1-D} \quad (38)$$

VI. RESULTS AND DISCUSSION

LTspice simulator was used to study the PSC-boost converter and its performance in split-phase control. Based on the simulation parameters in Table II, the two-level PSC-boost converter successfully converts 10V to 160V as presented in Figure 8.

TABLE II. SIMULATION PARAMETERS OF THE PSC-BOOST

Parameter	*Value*
Input voltage (V)	12V
Switching Frequency B_{oost} (kHz)	100
Switching Frequency S_1 to S_8 (kHz)	200
Diode type	MBRS240LT3
Switches type	IRFI540NPbF
C_1 to C_7	94µF
C_{f1}, C_{f2} and C_o	188µF
Duty cycle of S_{boost}	50%

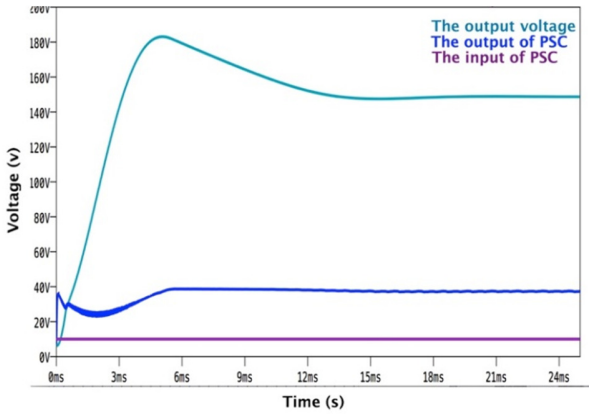

Fig. 8. The output voltage of the proposed PSC-boost converter.

Furthermore, the single inductor in the boost side was replaced by a switched inductor model to increase the proposed converter's gain and its rated output power. The switched-inductor cell operates in two operation modes regarding to the S_{boost} states. The three inductors have a parallel connection when S_{boost} is on and a series connection when S_{boost} is off. Having parallel and series connections allows inductors to charge and discharge instantaneously. The dependency between S_{boost} states and inductors' connections can be proven by the waveform similarity between the switched inductor input current and the S_{boost} gate driver, as indicated in Figure 9.

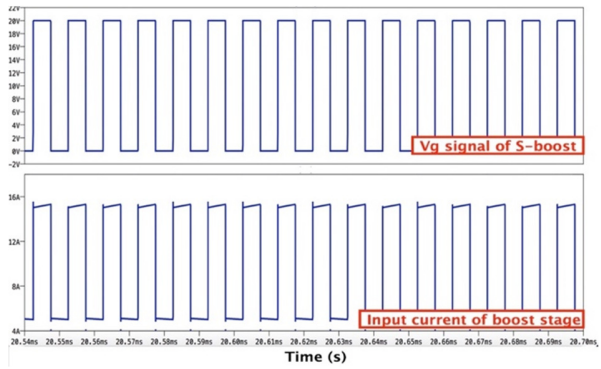

Fig. 9. I_{in} with the duty cycle, shows L_1, L_2 and L_3 parallel and series connections.

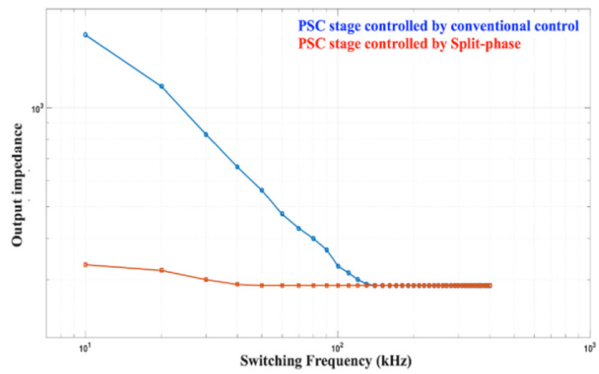

Fig. 10. The output impedance at two different control diagrams.

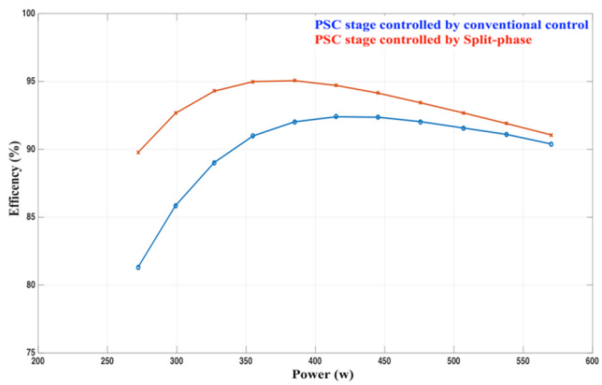

Fig. 11. The efficiency of PSC multiplier cells at two different control diagrams.

Since the PSC-boost converter consists of two stages (SC cells and a conventional DC-to-DC boost converter), in this

article the primary stage of PSC cells was designed to operate in the complete soft-charging operation [13, 15]. The complete soft-charging operation effectively reduces the switching frequency requirement that is essential to decrease the SC converter's output impedance as presented in Table I. However, in order to achieve the complete soft-charging operation, a split-phase control diagram is needed. The split-phase diagram presents a transition mode between any two existing modes in the conventional operation. For instance, a transition mode, called Mode-1b, will appear between Mode-1 and Mode-2. The difference between Mode-1 and Mode-1b is that Mode-1b has three capacitors instead of four. The isolation of the fourth capacitor reduces the total charge multipliers, and as a result, lower output impedance will be achieved.

The work in [14] has been completed in this paper. The PSC converter is controlled by the split-phase control diagram instead of its conventional operation. Figure 10 shows a comparison of the PSC converter's output impedance before and after using the split-phase control diagram. It can be clearly seen that using a split-phase control diagram helps to reduce the output impedance and as a result a lower switching frequency is required to reduce the capacitors' losses. In addition to the output impedance reduction and low switching frequency requirement, the spilt-phase operations increase the converter's efficiency. The reduction of the output impedance which represents the SC converter loss is behind the high efficiency achievement.

VII. CONCLUSION

The LTspice simulator has been used to design the proposed model and successfully produces a 160V from 10V input. The effect of using a split-phase control diagram to improve the efficiency of the PSC-boost converter was proven in this article. The spilt-phase control diagram reduces the switching loss and the output impedance. The split-phase control diagram was compared with the conventional control diagram in [9] and the efficiency effectively increased from 92% to 95%. This superior efficiency achievement is caused by the lower output impedance and dead time periods. In addition, the split-phase reduces the switching frequency required to reduce the output impedance of the PSC stage. This requirement can be achieved at a lower switching frequency limit when the split control diagram is used. Furthermore, the split-phase reduces the effect of the higher switching frequency in order to reduce the output impedance. This requirement can be instead achieved at a lower switching frequency.

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