Analyzing the Impact of Loop Parameter Variations on the Transient Response of Second Order Voltage-Switched CP-PLL

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Abstract-The analysis of the behavior of Charge Pump Phase-Locked Loop (CP-PLL) is a challenging task due to its mixed-signal architecture. Out of its two types, i.e. Current Switched CP-PLL (CSCP-PLL) and Voltage Switched CP-PLL (VSCP-PLL), the prior produces symmetrical pump currents, resulting in an appropriate transient performance to be analyzed. The loop parameters are important to set the gain, target frequency, and assure the stability of the system. The more important is the bandwidth of the loop, which is dependent on the loop filter parameters to perform stable operation and locking time. In this paper, the impact of loop parameter variations on the overall transient behavior of the system is investigated. It has been shown that loop parameters play an important role to ease the design of mixed-signal PLLs.

Keywords-charge pump PLL; voltage switched charge pump; transient analysis; loop parameter variation; behavioral model simulations

I. INTRODUCTION

The CP-PLL is a mixed-signal architecture (i.e. a combination of digital and continuous time components) [1]. It is an essential building block in a variety of applications ranging from Radio Frequency (RF) communication like FM modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and clock and data recovery, Doppler shift frequency, mobile and wireless communication, servo control systems, and smart system applications [2-6]. As detailed in [7], CP-PLL is a widely used subsystem due to its theoretical zero static phase shift, and is also one of the simplest and most effective PLL-design platforms.

The basic components of a CP-PLL are described in [1]. The CP-PLL works as a negative feedback device, in which its servo mechanism synchronizes the phase and frequency of divided feedback signal $\upsilon_{div}(t)$ produced by an oscillator with the phase and frequency of the reference signal $\upsilon_{ref}(t)$. The phase error between $\upsilon_{ref}(t)$ and $\upsilon_{div}(t)$ signals is detected by the digital Phase-Frequency Detector (PFD) which then commands the Charge Pump (CP) circuit to compensate the error signal by producing correction signal (in the form of current or voltage signal during this interval) [6]. As a result, a subsequent pulse width modulated current signal is produced by the combined PFD-CP operation, which is the supplied to the Loop Filter (LF) circuit to establish a fine-tuned quasi-dc signal, driving

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the Voltage Controlled Oscillator (VCO) to produce the output frequency [9].

A CP-PLL basically operates in nonlinear acquisition and tracking regions. It is unlocked in the acquisition region and works in a strongly nonlinear pull-in process, while in the tracking region, it is locked and follows the phase error variations within the [−2π, 2π] range [6, 10, 13]. There are two types of CP-PLL on the basis of its configuration, namely Voltage Switched Charge Pump (VSCP) and Current Switched Charge Pump (CSCP) [6, 8, 9, 12]. Most research attention has been given to the Current Switched Charge Pump (CSCP) PLL, as it ideally provides a symmetrical pump current, resulting in suitable transient response which is simpler and easier to be analyzed, as compared to that of Voltage Switched Charge Pump (VSCP) which delivers asymmetrical pump currents to the electrical load of the LF, resulting in varying gain of the control system and hence affecting its tracking ability. However, the cost-effective and simplified design of constant voltage source has made VSCP-PLL commercially popular among charge pump PLLs [9]. So far, various models and methods have been developed for the analysis of VSCP-PLL behavior but this field still requires qualitative research for more efficient modeling and result accuracy in order to facilitate modern communication and control systems with improved tracking performance and stability.

In this paper, analysis has been conducted to determine the way the variation in loop parameters affects the transient response of the 2nd order VSCP-PLL, using behavioral model simulations. The results are compared with those obtained from the linear transfer function model of VSCP-PLL in the locked state to further verify its validation for the analysis of VSCP behavior.

II. THE PECULIAR EFFECT IN THE VSCP-PLL ARCHITECTURE

The CP-PLL is one of the most utilized circuits in frequency synthesis function. Due to the design simplicity of charge-pump, VSCP-PLL architecture is preferred in most applications. The VSCP introduces a peculiar effect in the form of non-constant current $i_p(t)$:

$$i_p(t)=\begin{cases}\dfrac{V_{DD}-\upsilon_{c1}(t)}{R_0+R_1} & \rightarrow UP\\ 0 & \rightarrow NULL\\ \dfrac{V_{SS}-\upsilon_{c1}(t)}{R_0+R_1} & \rightarrow DN\end{cases} \quad (1)$$

Since the gain of the phase detector is associated with the pump current, thus it affects the overall loop gain of the system [8]. Moreover, the engineers prefer the parameters of the linear model. The prediction of the system behavior of the CP-PLL is based on the following assumptions:

First of the all, the CP-PLL is under locked condition, thus the phase error is between [0, 2π] and PFD is in the linear range. Second, the output transfer characteristics of the VCO are considered linear over the tuning range. Considering these conditions, the Linear Time Invariant (LTI) system is represented with the transfer function, which is enough to predict the average behavior of the system:

$$H^{vs}(s)=\frac{\phi_{div}(s)}{\phi_{ref}(s)}=\frac{\omega_n^{vs}s\left(2\zeta^{vs}-\frac{\omega_n^{vs}}{\frac{K_vV_{DD}}{2N}}\right)+\omega_n^{vs^2}}{s^2+2\zeta^{vs}\,\omega_n^{vs}s+\omega_n^{vs^2}} \quad (2)$$

Generally, two parameters (ζ, ω_n) are important to predict the system behavior using the linear approach:

$$\omega_n^{vs}=\sqrt{\frac{K_vV_{DD}}{2N(R_0+R_1)C_1}}$$
$$\zeta^{vs}=\frac{\omega_n^{vs}}{2}\left[\tau_1+\frac{1}{\frac{K_vV_{DD}}{2N}}\right] \quad (3)$$

The value of ζ^{vs} is not the same as of ζ for the current switched CP-PLL as given in [10]. The linear model represented by (2) is only valid in the locked state. If the output frequency deviates from the center frequency due to frequency excursions or non-linear function of the VCO characteristics, then the linear representation may not be efficient enough to predict non-linearities at even a small scale. Therefore, the impact of such peculiar effect complicates the analysis of VSCP-PLL systems. Thus, more rigorous approaches may be required for analyzing the weakness of such systems in following the ramping system behavior. One of the best approaches apart from the circuit level are the behavioral modeling of such system [10, 11], which can be sufficient to predict non-linear acquisition region of such complex system.

III. TRANSIENT ANALYSIS OF 2ND ORDER VSCP-PLL

The P-PLL has a non-linear switching behavior and is initial condition dependent. Generally, the CP-PLL operates in two regions, non-linear acquisition region (during unlocking) and tracking region (during locking). Stable PLL operation may be predicted by the transfer function model if the following condition is true:

$$\frac{\omega_{ref}^{vs}}{\omega_n^{vs}}\geq 10 \quad (3)$$

The sampling ratio in the pulse width modulated behavior of VSCP-PLL is set by (3) [14]. Generally the information is hidden in two parameters: damping factor (ζ) and natural angular frequency (ω_n) ,which can be sufficient and a starting point toward the stability condition [15]. A set of parameters was chosen to perform behavioral simulations in SIMULNIK. The transient behavior (in symmetrical condition during locking) of a second order VSCP-PLL is shown in Figure 1. The symmetrical condition is only obtained when $\upsilon_{ctr}(t)=V_{DD}/2$.

A. Loop Parameter Variations (Changing N)

The VSCP-PLL loop is defined by parameters designed to achieve stability and suitable transient characteristics. A VSCP-PLL can be used as a frequency synthesizer; the divider circuit is implemented to perform this function. It can be difficult to design multiband VCO, thus by changing the value of *N*, the output frequency response that targets voltage can be changed easily. It can be observed that the slope of the rising voltage over the input of the VCO is not constant as a consequence of the weak dynamics of VSCP-PLL due to the non-constant pump current.

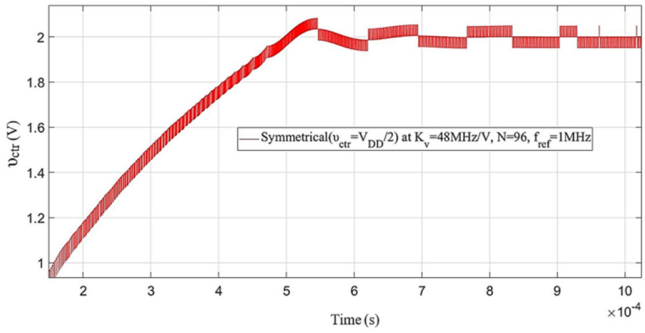

Fig. 1. Symmetrical transient behavior of the VSCP-PLL.

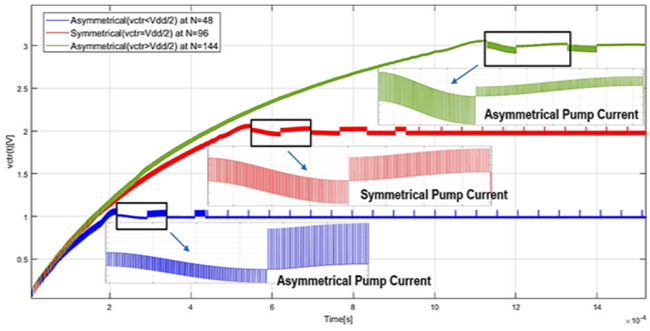

Fig. 2. The transient simulations by changing *N*.

B. Loop Parameter Variations (Changing K_v)

As discussed in the above subsection, it can be difficult to change the gain of the VCO (K_v), or implement multiband VCOs. The occurrence of non-linearities may impact the transient or steady state of the VSCP-PLL and may cause the system to unlock at any stage. Thus, in behavioral simulations it may be easy to change the K_v, however this is quite challenging during the design process. By changing the gain, the target voltage is changed in a similar way as changing the *N* under the locked condition:

$$\upsilon_{\text{target}}(t) = \frac{f_{\text{ref}} \times N}{K_{\text{v}}} \quad (4)$$

From (4), it is easy to predict that the transient behavior can be changed by changing the linear gain (K_v) of the VCO or *N*. Similarly, it can be observed that the VSCP-PLL exposes its asymmetrical behavior during non-linear pull in process during locking, as it is evident from the voltage steps during the UP and DN cycles (Figure 3). The target frequency can be changed either by changing *N* or K_v. Since the divider can be programmable, therefore it is more easier to modulate *N*. Obviously, when the CSPL-PLL system is locked at different target frequencies, the transient parameters like rise time (t_r), peak time (t_p), percent overshoot and settling time (t_r) vary. The two dynamic time parameters given in Table I show how the response is changing when the system is locked in symmetrical or asymmetrical condition. Moreover, the linear and behavioral model parameters are constant when the system is locked under symmetrical conditions, however these parameters divert when considering the symmetrical situation. It can be concluded that, the linear model is only valid in the symmetrical condition for a second order VSCP-PLL unlike CSCP-PLL.

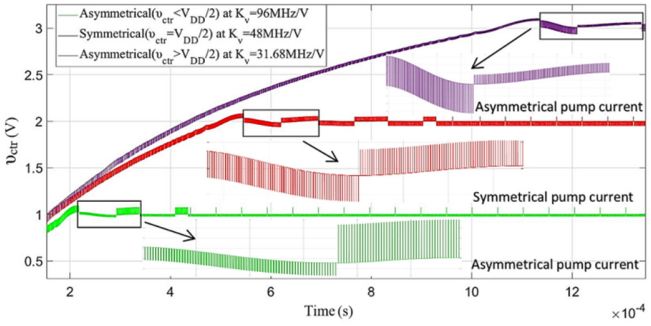

Fig. 3. The transient simulations for different values of K_v.

TABLE I. TRANSIENT PARAMETER VARIATION AT DIFFERENT K_V WITH SYMMETRICAL AND ASYMMETRICAL BEHAVIOR

Transient parameter	Linear model (theoretical)	Behavioral model
At K_v=48MHz/V ($\upsilon_{ctr}(t) = \frac{V_{DD}}{2}$) ζ^{vs}=0.3070, ω_n^{vs}=4.3853x10^4 rad/s, $\frac{\omega_{ref}^{vs}}{\omega_n^{vs}}$= 143.2787		
t_p	75.2 us	74 us
t_r	45.1 us	45 us
At K_v=96MHz/V ($\upsilon_{ctr}(t) < \frac{V_{DD}}{2}$) ζ^{vs}=0.4186, ω_n^{vs}= 6.2017x10^{4}rad/s, $\frac{\omega_{ref}^{vs}}{\omega_n^{vs}}$= 101.3133		
t_p	55.7 us	47 us
t_r	35.5u s	32 us
At K_v=31.68MHz/V ($\upsilon_{ctr}(t) > \frac{V_{DD}}{2}$) ζ^{vs} = 0.2586, ω_n^{vs}= 3.5626 x10^4 rad/s, $\frac{\omega_{ref}^{vs}}{\omega_n^{vs}}$= 176.3639		
t_p	91.286 us	126 us
t_r	53.24 us	52 us

C. Loop Filter Parameter Variations

The LF parameters are important in obtaining stable system operation, as the overall bandwidth and damping of the system is related to the LF parameters. Moreover, there is residual damping due to the inclusion of the VSCP architecture.

1) Impact of Changing R_1 on Transient Response

The transient response of the 2nd order VSCP-PLL for various values of R_1 at symmetrical condition of the charge-pump voltage, is shown in Figure 4. It can be observed that the speed of response is affected and the system behavior is more damped as the value of R_1 is increasing (Figure 5). It is worth noting that when the R_1 is set to zero the system expanses its weakly damped response. It is evident from (3) that the system has residual damping due to the VSCP structure. Changing R_1 has a slight impact on the natural frequency of the system.

2) Impact of Changing C_1 on Transient Response

The LF parameters are very important in establishing the quasi-dc voltage at the input of the VCO in order to produce a signal proportional to the control voltage. The time constant of the LF cirucit sets the speed of the VSCP-PLL which highly impacts transient parameters like rise time and locking time. As

shown in Figures 5-6, the transient simulation varies due to the variation of C_1. The time constant is increasing and the natural angular frequency of the system is decreasing. However, there is less impact on the damping of the system.

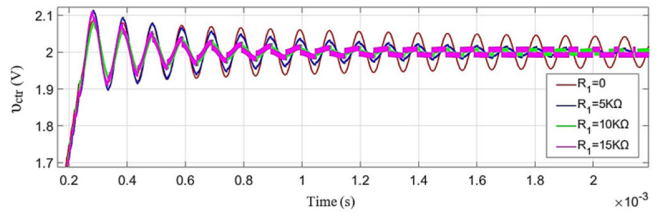

Fig. 4. Transient behavior of VSCP-PLL at different values of R_1 (V_{DD}=4V, R0=2MΩ, f_{ref}=1MHz, N=96, K_v=48MHz/V, $R1$=10KΩ, R_1=0, 5KΩ ,10KΩ and 15KΩ).

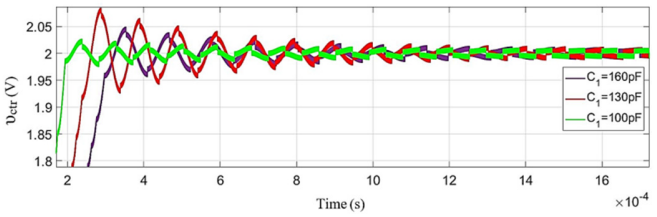

Fig. 5. Transient behavior of VSCP-PLL at different values of C_1 (V_{DD}=4V, $R0$=2MΩ, f_{ref}=1MHz, N=96, K_v=48MHz/V, R1=10KΩ, C_1=100pF, 130pF, and 160pF).

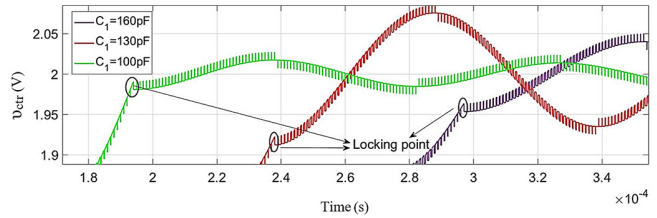

Fig. 6. Impact of varying capacitor C_1 of the LF on the locking time of VSCP-PLL.

IV. CONCLUSION

In this paper, the impact of variations in loop parameters (K_v, N, and τ) on the VSCP-PLL's transient behavior was investigated using behavioral simulations. The results revealed that the change in the divider ratio N and VCO gain K_v has direct impact on the overall transient characteristics as the loop gain is associated to charge pump current. By changing N and K_v, the locking time and the natural angular frequency ω_n^{vs} of the system vary. Moreover, changing the values of C_1 of the LF circuit under symmetrical pump current, also affects the ω_n^{vs} whereas varying the values of R_1 of the LF circuit has little impact on the ω_n^{vs} and the locking time of VSCP-PLL, however, it has significant influence on system's damping response. These parameters highly affect the system's transient characteristics such as rise time and peak. It was also shown that a VSC-based system exhibits weakly damped behavior even when the R_1 is set to zero, unlike the CSCP based system [8], however, it leads to improved system stability [15].

REFERENCES

[1] B. A. A. Antao, F. M. El-Turky, and R. H. Leonowich, "Behavioral modeling phase-locked loops for mixed-mode simulation," *Analog Integrated Circuits and Signal Processing*, vol. 10, no. 1, pp. 45–65, Jan. 1996, https://doi.org/10.1007/BF00713978.

[2] Gardner, *Phaselock Techniques, 3rd Edition*, 3rd ed. Hoboken, NJ, USA: Wiley-Interscience, 2005.

[3] R. E. Best, *Phase-Locked Loops : Design, Simulation, and Applications*, 5th ed. New York, NY, USA: McGraw-Hill Professional, 2003.

[4] D. M. Perisic and M. Bojovic, "Application of Time Recursive Processing for the Development of a Time/Phase Shifter," *Engineering, Technology & Applied Science Research*, vol. 7, no. 3, pp. 1582–1587, Jun. 2017, https://doi.org/10.48084/etasr.1179.

[5] H. E. Taheri, "A 4-4.8GHz Adaptive Bandwidth, Adaptive Jitter Phase Locked Loop," *Engineering, Technology & Applied Science Research*, vol. 7, no. 2, pp. 1473–1477, Apr. 2017, https://doi.org/10.48084/etasr.1099.

[6] E. Ali, G. Bhutto, K. Amur, N. Nizamani, R. Khatri, and T. Memon, "Non-linear model of the second order voltage and current switched CP-PLLs," *Sindh University Research Journal*, vol. 45, no. 4, pp. 737–742, 2013.

[7] P. K. Hanumolu, M. Brownlee, K. Mayaram, and Un-Ku Moon, "Analysis of charge-pump phase-locked loops," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 9, pp. 1665–1674, Sep. 2004, https://doi.org/10.1109/TCSI.2004.834516.

[8] C. Hangmann, C. Hedayat, and U. Hilleringmann, "Designing Mixed-Signal PLLs regarding Multiple Requirements taking Non-Ideal Effects into Account," in *2019 17th IEEE International New Circuits and Systems Conference (NEWCAS)*, Munich, Germany, Jun. 2019, pp. 1–4, https://doi.org/10.1109/NEWCAS44328.2019.8961261.

[9] E. Ali, C. Hangmann, C. Hedayat, F. Haddad, W. Rahajandraibe, and U. Hilleringmann, "Event Driven Modeling and Characterization of the Second Order Voltage Switched Charge Pump PLL," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 3, pp. 347–358, Mar. 2016, https://doi.org/10.1109/TCSI.2015.2512759.

[10] F. Gardner, "Charge-Pump Phase-Lock Loops," *IEEE Transactions on Communications*, vol. 28, no. 11, pp. 1849–1858, Nov. 1980, https://doi.org/10.1109/TCOM.1980.1094619.

[11] C. D. Hedayat, A. Hachem, Y. Leduc, and G. Benbassat, "Modeling and Characterization of the 3rd Order Charge-Pump PLL: a Fully Event-driven Approach," *Analog Integrated Circuits and Signal Processing*, vol. 19, no. 1, pp. 25–45, Apr. 1999, https://doi.org/10.1023/A:1008326315191.

[12] E. Ali, W. Rahajandraibe, F. Haddad, C. Hedayat, and C. Hangmann, "Simulative characterization of the stability for second order voltage switched CP-PLL," in *2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Columbus, OH, USA, Aug. 2013, pp. 153–156, https://doi.org/10.1109/MWSCAS.2013.6674608.

[13] N. Margaris and V. Petridis, "Voltage Pump Phase-Locked Loops," *IEEE Transactions on Industrial Electronics*, vol. IE-32, no. 1, pp. 41–49, Feb. 1985, https://doi.org/10.1109/TIE.1985.350140.

[14] D. Dhar, P. T. M. van Zeijl, D. Milosevic, H. Gao, and P. G. M. Baltus, "Analysis of the Effect of PFD Sampling on Charge-Pump PLL Stability," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, May 2018, pp. 1–5, https://doi.org/10.1109/ISCAS.2018.8351180.

[15] A. Mansukhani, "Phase lock loop stability analysis," *Applied Microwave and Wireless*, vol. 12, no. 2, pp. 30–41, 2000.