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SPICE MODELING OF IONIZING RADIATION EFFECTS IN CMOS DEVICES

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Abstract. *Electric characteristics of devices in advanced CMOS technologies change over the time because of the impact of the ionizing radiation effects. Device aging is caused by cumulative contribution of generation of defects in the gate oxide and/or at the interface silicon-oxide. The concentration of these defects is time and bias-dependent values. Existing models include these effects through constant shift of voltage threshold. A method for including ionizing radiation effects in Spice models of MOS transistor and FinFET, based on an auxiliary diode circuit using for derivation of values of surface potential, that also calculates the correction time-dependent voltage due to concentration of trapped charges, is shown in this paper.*

Key words: *Ionizing radiation effects, Trapped charges, Spice model, CMOS devices*

1. INTRODUCTION

With aggressive scaling of device dimensions in CMOS technologies, which includes the decrease of oxide thickness and the increase of doping concentration in the channel, the susceptibility of the most CMOS technologies has been reduced. Scaling of the oxide thickness caused the decrease of concentration of fixed charge in the oxide, because the value of the concentration is directly proportional to the oxide thickness. On the other side, the increase of doping concentration in the channel decreased the oxide trapped charge effect on the surface potential of the channel, which also caused robustness of the components on ionizing radiation [1]. However, recent studies showed that the negative bias temperature instability damage and hot carrier injection damage were attributed to the charges trapped in the oxide (with areal density N_{ox}) and/or at the interface of the silicon and oxide layers (with energy density distribution D_{it}) [2-4]. Therefore, trapped charges still represent a potential radiation threat and have measurable impact on the integrated circuits performances [2,5].

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A harmful effect of ionizing radiation on CMOS devices can be diminished by using well-known techniques, such as radiation-hardening-by-process (RHBP) and radiation-hardening-by-design (RHBD) techniques [6,7]. However, even with significant efforts in RHBP and RHBD techniques, the capability of estimating the influence of ionizing radiation on electric characteristics of devices in advanced technologies are still improper [8]. Analysing of test IC circuits on ionizing radiation is quite expensive [7], so the incorporation of ionizing radiation effects in devices compact models used in standard electric circuits simulators is put upon as an alternative. The incorporation of these effects needs the knowledge of physical processes which contribute to emerging of the defects due to ionizing radiation and the impacts which these effects have on the electric characteristics of components in advanced CMOS technologies [8,9]. Numerous existing techniques for modelling these effects in circuit simulators are based on the fixed change of threshold voltage (threshold voltage shift), not considering the special impact which these defects have on the electric characteristics of the transistors [2,10-12].

Previously derived surface-potential based non-quasi static MOS model (NQS MOS model) and non-quasi static SOI model (NQS SOI model) can be modified as to include these effects of oxide trapped charges and interface trapped charges is described in this paper [13,14].

2. IONIZING RADIATION EFFECTS IN CMOS DEVICES

The main cause of the damage that occurs in CMOS devices after ionizing radiation is the generation of the electron-hole pairs in the oxide (or another dielectric) as a material that is the most sensitive to ionizing radiation in CMOS devices. After the generation of the electron-hole pairs, some of the pairs are immediately recombined. Since the electron mobility in the oxide is considerably bigger that the hole mobility [15,9], the electrons will be soon swept out of the oxide or the dielectrics, while the holes will move slowly through the oxide to the interface SiO_2-Si, causing long-term effects of the ionizing radiation. Fig. 1 shows the processes after the ionizing radiation.

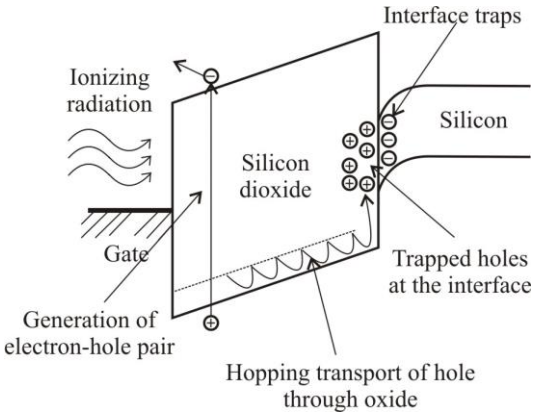

Fig. 1 Processes in the oxide after the ionizing radiation [16]

Vacancies in the oxide or the dielectrics can trap the generic holes. A total amount of trapped charge in the oxide is N_{ox}. The trapped charge changes the threshold voltage V_{th} of CMOS devices for the threshold voltage shift [17]:

$$\Delta V_{th} = -\frac{q\, t_{ox}^2\, N_{ox}}{\varepsilon_{ox}}, \tag{1}$$

where q is the electron charge, t_{ox} is the oxide thickness and ε_{ox} is the oxide permittivity. The threshold voltage shift ΔV_{th} is negative, which means that in the case of the NMOS transistor the off current increases, while in the case of the PMOS transistor the total value of threshold voltage V_{th} increases, as shown in Fig. 2(a). It can be concluded from (1) that ΔV_{th} depends on the square of the oxide thickness; with the decrease of the oxide thickness in nanometer CMOS technologies and due to the change of the threshold voltage the oxide trapped charge will be smaller.

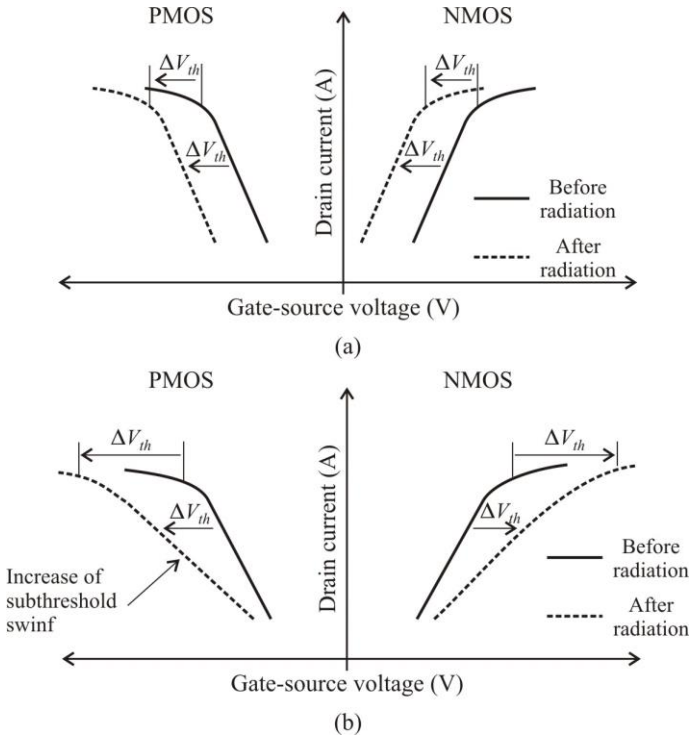

Fig. 2 Illustration of the threshold voltage shift V_{th} due to the oxide trapped charges (a) and increase in subthershold swing due to interface trapped charges (b) [17]

After the ionizing radiation, the generation of interface traps occurs, which concentration is N_{it}. The generation holes react with hydrogen atoms in the oxide, making in such a way H^+ ions [18]. These ions move by drifting to SiO_2-Si interface, and create

dangling bonds (i.e. Pb centres) [2]. Interface trapped charges are often linked with the permanent effects of components aging [2,10].

Fig. 2(b) shows the impact of the generation of trapped charges at the SiO_2-Si interface on the transfer characteristic of the transistors. It can be noted that these charges increase the swing in the device subthreshold region. For NMOS and PMOS transistors, the generation of interface trapped charges decreases the transistor off current.

3. NQS MOS AND NQS SOI TRANSISTOR MODELS

Static and dynamical characteristics of transistors can be described by set of basic equations, which are comprised of Poason's equation, drift-diffusion and continuity equations [19]. Since MOS transistor modelling is three dimensional problem, solving these sets of equations is complex and memory demanding. However, for numerous practical applications of MOS transistors, changes in the third direction can be neglected and problem can be reduced to two dimensional problem (to *x* and *y* direction).

3.1. NQS MOS transistor model

In [13] a physically based NQS MOS transistor model is described, which belongs to a group of models based on surface potential. Fig. 3 shows equivalent model scheme, which as a subcircuit can be embedded into electric circuit simulators. External elements of transistor model (resistors and capacitors) can be modelled in a similar way as in other stationary or non-stationary models.

Unlike some known models [20-22], in the NQS MOS model there are no analytical expressions for node currents, but they are obtained after the solution of equivalent circuit shown on Fig. 3(a). This subcircuit has two parts, as shown on Fig. 3(b):

- Internal part is connected to transistor gate terminal. This part of the model is, in fact, equivalent line that models drift-diffusion transport of electrons in transistor channel;
- External part is connected to source, drain and gate terminals, and it contains current-controlled current sources i_{S1} and i_{SN}. This part of the circuit is defined by the potential of source, drain and substrate that is obtained by mirroring the currents which flow through voltage sources ϕ_{S1} and ϕ_{SN}.

Voltage generators ϕ_{S1} and ϕ_{SN} copy values of boundary surface potentials to subcircuit in the source end and the drain end of channel.

Voltage generator V_B serves to copy bulk polarisation to equivalent subcircuit. Capacitance C_{oxk} represents gate-oxide capacitance ($C_{oxk} = C_{ox} / N$). The other model elements R_k and C_k, non-linear channel resistance and depletion region capacitance, are respectively defined by the equations:

$$R_k = \frac{(1+A_1(V_{GS}-\phi_{Sk}))+(1+(A_2(\phi_{Sk+1}-\phi_{Sk}))^{A_3})^{1/A_3}}{A_4\ \left|A_5(V_{GB}-V_{fb}-\phi_{Sk})-A_6\sqrt{\phi_{Sk}}\right|}, \tag{2}$$

$$C_k = \left|\frac{\partial\ Q_{bk}}{\partial\phi_{Sk}}\right| = \sqrt{\frac{\varepsilon_0\varepsilon_{Si}qN_{ch}}{2\phi_{Sk}}} = A_7(\phi_{Sk})^{-1/2}, \tag{3}$$

where the constants $A_1 \div A_7$ are physically based, N_{ch} is doping concentration in the channel and ε_{Si} is the silicon permittivity. Surface potential of every cell is denoted with ϕ_{Sk}. The derivations for (2) and (3) and the expressions for $A_1 \div A_7$ are given in [13].

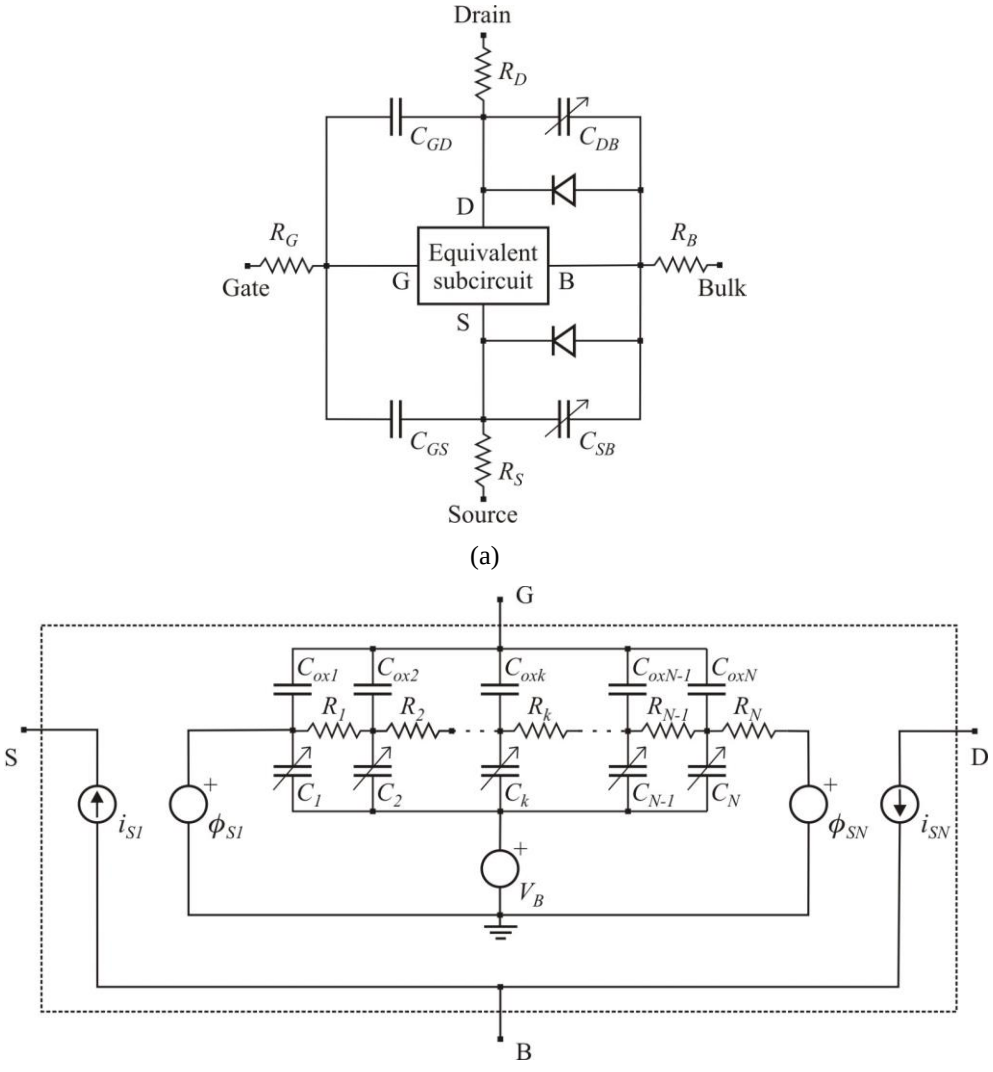

Fig. 3 NQS MOS model (a) and the equivalent subcircuit (b)

In a surface charge-sheet model, which describes MOS transistor operation [23], the boundary channel potentials ϕ_{S1} and ϕ_{SN} at the source and drain side are functions of biasing voltage of transistor terminals through the following recurrent relations [24]:

$$\phi_{S1} = 2\phi_f + V_{SB} + V_T \quad \ln\left\{\frac{1}{V_T}\left(\frac{1}{\gamma^2}(V_{GB} - V_{fb} - \phi_{S1})^2 - \phi_{S1}\right)\right\}, \tag{4}$$

$$\phi_{SN} = 2\phi_f + V_{SB} + V_{DS} + V_T \quad \ln\left\{\frac{1}{V_T}\left(\frac{1}{\gamma^2}(V_{GB} - V_{fb} - \phi_{SN})^2 - \phi_{SN}\right)\right\}. \tag{5}$$

In the previous equations γ is the body factor, V_T is the thermal voltage, ϕ_f is the channel potential ($=V_T \ln(N_{ch}/n_i)$) and V_{fb} is the flatband voltage. Since the equations (4) and (5) are implicit relations, to determine surface potentials ϕ_{S1} and ϕ_{SN} there are several iterative methods proposed in the literature [25]. In the NQS MOS model, relations (4) and (5) are determined by diode circuits. For any point y in the channel is:

$$\exp(\phi_{Sy}/V_T) - 1 = \exp(2\phi_{fy}/V_T) \cdot \left\{\frac{1}{V_T}\left(\frac{1}{\gamma^2}(V_{GB} - V_{fb} - \phi_{Sy})^2 - \phi_{Sy}\right)\right\} - 1. \tag{6}$$

By comparing the equation (6) with the diode current expression:

$$I_d = I_0(\exp(\phi_{Sy}/V_T) - 1) = I_{ss} \tag{7}$$

the conclusion is that:

$$\begin{aligned} I_{ss} &= \exp(2\phi_{fy}/V_T) \cdot \left\{\frac{1}{V_T}\left(\frac{1}{\gamma^2}(V_{GB} - V_{fb} - \phi_{Sy})^2 - \phi_{Sy}\right)\right\} - 1, \\ I_0 &= 1. \end{aligned} \tag{8}$$

When determining the boundary surface source potential ϕ_{S1}, in the equation (8) ϕ_{Sy} and ϕ_{fy} should be replaced with $\phi_{Sy} = \phi_{S1}$ and $\phi_{fy} = 2\phi_f + V_{SB}$, consecutively, while for determining boundary surface potential on the drain side ϕ_{SN} instead ϕ_{Sy} and ϕ_{fy} should be used ϕ_{SN} and $2\phi_f + V_{SB} + V_{DS}$, respectively. Owning to this type of analysis, it is possible to construct a circuit for solving equations (7) and (8), which is comprised of a diode (with unit current $I_0 = 1$) and voltage-controlled current source, where the current is calculated by the equation (8). Figure 4 shows this type of auxiliary diode circuit.

For determining both boundary surface potentials, ϕ_{S1} and ϕ_{SN}, there are used two identical diode subcircuits and the described method is used to solve the equations (4) and (5). The values of the boundary surface potentials determined in this way are copied with voltage generators ϕ_{S1} and ϕ_{SN} (shown in Fig. 3(b)) on the input and output of equivalent circuit to solve the transport of the electrons in the channel. Knowing the boundary surface potentials allows us to calculate the values of nonlinear resistors and capacitors R_k and C_k, namely to determine the transistor currents.

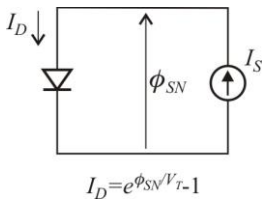

Fig. 4 Diode subcircuit for solving surface potentials

A physical base of the NQS MOS model in an easy way allows including significant effects shown in aggressive scaling of transistor dimensions, like, for example, short channel effects and quantum-mechanics effects.

3.2. NQS SOI transistor model

A compact model for n-channel fully depleted SOI MOS transistor with double gate (FD SOI transistor) is developed based on the NQS MOS model, and it is applicable for asymmetrical and symmetrical planar structures [14]. In non-stationary model of FD SOI MOS transistor (NQ SOI model), a transistor is represented by parallel connection of two SOI transistors with one gate, as shown in Fig. 5, to model current in a front and back channel [14].

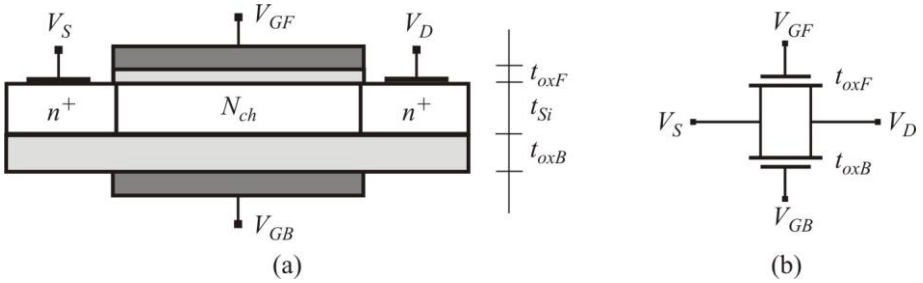

Fig. 5 Schematic presentation of FD SOI transistor (a) and its electric equivalent (b)

By comparison with the NQS MOS model, recurrent expressions for calculating boundary surface potentials in the NQ SOI model also contains the influence of biasing of both gates. So the boundary surface potentials in channel ϕ_{S1} and ϕ_{SN} in the FD SOI transistor are connected with biasing of front (V_{GF}) and back (V_{GB}) gate, and biasing between drain and source V_{DS} with new recurrent relations [26,27]:

$$\frac{1}{\gamma^2}\left[(V_{GF}-V_{fbF}-\phi_{S1})^2-\frac{t_{oxF}^2}{t_{oxB}^2}(V_{GF}-V_{fbB}-\phi_{B1})^2\right]= \tag{9}$$
$$V_T e^{-2\phi_f/V_T}(e^{\phi_{S1}/V_T}-e^{\phi_{B1}/V_T})+V_T(e^{-\phi_{S1}/V_T}-e^{-\phi_{B1}/V_T})+\phi_{S1}-\phi_{B1},$$

$$\frac{1}{\gamma^2}\left[(V_{GF}-V_{fbF}-\phi_{Sn})^2-\frac{t_{oxF}^2}{t_{oxB}^2}(V_{GF}-V_{fbB}-\phi_{Bn})^2\right]= \tag{10}$$
$$V_T e^{-(2\phi_f+V_{DS})/V_T}(e^{\phi_{Sn}/V_T}-e^{\phi_{Bn}/V_T})+V_T(e^{-\phi_{Sn}/V_T}-e^{-\phi_{Bn}/V_T})+\phi_{Sn}-\phi_{Bn},$$

where, in the case of fully depleted silicon layer, boundary potentials of back channel can be expressed as:

$$\phi_{B1}\approx\phi_{S1}-\frac{q\,N_{ch}\,t_{Si}^2}{\varepsilon_{Si}} \quad \text{and} \quad \phi_{Bn}\approx\phi_{Sn}-\frac{q\,N_{ch}\,t_{Si}^2}{\varepsilon_{Si}}, \tag{11}$$

while for a fully symmetrical transistor applies $t_{oxF} = t_{oxB}$. In the equations (9)-(11) the index F relates to the front gate, and the index B relates to the back gate. Recurrent

relations (9) and (10) are calculated with the assumption that the difference of Fermi's potentials between the source and the drain is equal to the voltage V_{DS}. Electric potential distribution in the channel through depth, i.e. in the line of axis x, is obtained by solving these recurrent relations (Fig. 6).

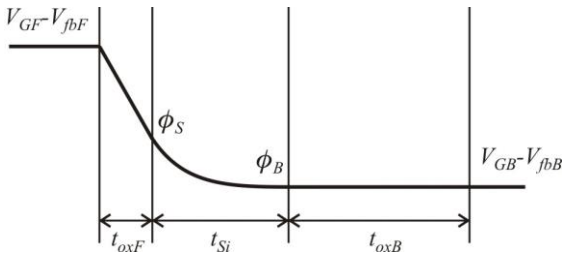

Fig. 6 Electric potential distribution in the channel through depth of FD SOI transistor

For applications in the NQ SOI model for a symmetrical FD SOI MOS transistor, recurrent equations for calculating boundary surface potentials can be written with basic algebraic transformations [14] in the following form:

$$I_{S1}(e^{\phi_{Sx}/V_T}) + I_{S2}(e^{-\phi_{Sx}/V_T}) = I_S, \tag{12}$$

while:

$$I_S = \frac{1}{V_T}\left\{\frac{1}{\gamma^2}\left[(V_{GF} - V_{fbF} - \phi_{Sx})^2 - \left(V_{GF} - V_{fbB} - \phi_{Sx} + \frac{qN_{ch}t_{Si}^2}{\varepsilon_{Si}}\right)^2\right] - \frac{qN_{ch}t_{Si}^2}{\varepsilon_{Si}}\right\}, \tag{13}$$

$$I_{S1} = e^{-\phi_{fx}/V_T}\left(1 - \exp\left(-\frac{q\,N_{ch}\,t_{Si}^2}{V_T\,\varepsilon_{Si}}\right)\right), \tag{14}$$

$$I_{S2} = 1 - \exp\left(\frac{q\,N_{ch}\,t_{Si}^2}{V_T\,\varepsilon_{Si}}\right), \tag{15}$$

where on the source side $\phi_{Sx} = \phi_{S1}$ and $\phi_{fx} = 2\phi_f$, while on the drain side the changes have to be made $\phi_{Sx} = \phi_{Sn}$ and $\phi_{fx} = 2\phi_f + V_{DS}$. In the previous expressions, t_{Si} is the silicon film (body) thickness. Auxiliary diode circuits, similar to the NQS MOS model for solving recurrent relations, are used in this way for calculating boundary values of surface potentials in the NQ SOI model. Fig. 7 shows equivalent diode circuit for solving the equation (12) [14].

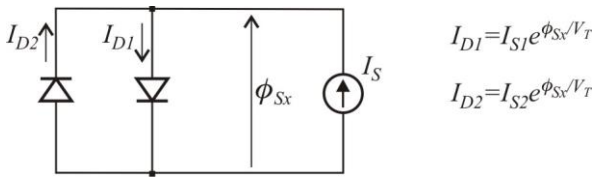

Fig. 7 Diode subcircuit for solving surface potentials in NQS SOI model

4. INCLUSION OF N_{OX} AND D_{IT} IN NQS MOS AND NQS SOI MODELS

A physical foundation of previously described models allows easily inclusion of effects important for transistor operation. Modelling of the effects of generation interface trapped charge with energy density distribution D_{it} and oxide trapped charge with areal density N_{ox} is possible in NQS MOS and NQS SOI model by changing the surface potential equations. It is possible to model the impact of these effects onward on the characteristics of transistor in two ways:

1. Auxiliary diode circuits, with the included effects of N_{ox} and D_{it}, are used for determining surface potentials for use in NQS MOS and NQS SOI models or
2. Auxiliary diode circuits, with the included effects of N_{ox} and D_{it}, are used for determining surface potentials, and then to connect consecutively to gate of some standard models (for example, BSIM 4 for MOS transistor or BSIM.CMG for FinFET).

A total amount of electric charge caught in oxide is:

$$Q_{ox} = qN_{ox}, \tag{16}$$

while a total amount of interface charge [19]:

$$Q_{it} = q\int_{E_F}^{E_g/2} D_{it}\cdot dE_{it} = qD_{it}\left(\frac{E_g}{2} - E_f\right), \tag{17}$$

where $E_g / 2$ is the midgap energy level at the interface and E_f is the energy of Fermi level. If we add and subtract the factor $E_{gb} / 2$, where E_{gb} is the bulk midgap energy level, to the factors in the equation parenthesis (17) we have:

$$\begin{aligned} Q_{it} &= qD_{it}\left(\frac{E_g}{2} - \frac{E_{gb}}{2} - E_f + \frac{E_{gb}}{2}\right) \\ &= -qD_{it}\left[\left(\frac{E_{gb}}{2} - \frac{E_g}{2}\right) - \left(\frac{E_{gb}}{2} - E_f\right)\right] \\ &= -qD_{it}\left(\phi_S - \phi_f\right). \end{aligned} \tag{18}$$

As stated in the Section 2, charges Q_{ox} and Q_{it} have impact on the change of the transistor voltage threshold. This change can be expressed by correction potential ϕ_{nt} [6]:

$$\phi_{nt} = \frac{Q_{ox} + Q_{it}}{C_{ox}} = \frac{q}{C_{ox}}[N_{ox} - D_{it}(\phi_S - \phi_f)]. \tag{19}$$

In the NQS MOS model, the equations (4)-(6) are modified in a way to include correction potential ϕ_{nt}. Eqn. (6) in a modified form with included correction potential is:

$$\exp(\phi_{Sy}/V_T) - 1 = \exp(2\phi_{fy}/V_T)\cdot\left\{\frac{1}{V_T}\left(\frac{1}{\gamma^2}(V_{GB} - V_{fb} - \phi_{Sy} + \phi_{nt})^2 - \phi_{Sy} + \phi_{nt}\right)\right\} - 1. \tag{20}$$

For determining surface potential ϕ_{Sy}, two identical diode circuits are used, as shown in Fig. 3(b).

In the NQS SOI model, for a symmetrical FD DG SOI transistor, the equation for surface potential is modified in a way to include ϕ_{nt} in the following way:

$$\begin{aligned}&\frac{1}{\gamma^2}\left[(V_{GF}-V_{fbF}+\phi_{nt}-\phi_{S1})^2-(V_{GF}-V_{fbB}+\phi_{nt}-\phi_{B1})^2\right]=\\&V_T e^{-(2\phi_f+bV_{DS})/V_T}(e^{\phi_{S1}/V_T}-e^{\phi_{B1}/V_T})+V_T(e^{-\phi_{S1}/V_T}-e^{-\phi_{B1}/V_T})+\phi_{S1}-\phi_{B1}.\end{aligned} \tag{21}$$

The parameter b, which appears in the equation (21), can have the value $b = 0$ for the source end of the channel and $b = 1$ for the drain end of the channel (in accordance with the equations (9) and (10)). However, the main problem in modelling of trapped charges with (21) is the fact that the distribution of surface potential in the channel depends not only on gate voltage, but also on drain voltage V_{DS} due to split of quasi Fermi levels [19]. It means that the concentration Q_{it} will change along the channel, even for the constant N_{it}. The impact of the changeable charge Q_{it} along the channel can be modelled with a modified value of the parameter $b \in (0,1)$. In the equation (21) it is calculated with in advance known value, and it is possible with the fine tuning [28] to accomplish better match of the model results with the results of 2D TCAD numeric simulator Silvaco Atlas [29].

The equation (21) can also be solved with auxiliary diode circuits (Fig. 7) with:

$$I_S=\frac{1}{V_T}\left\{\frac{1}{\gamma^2}\left[(V_{GF}-V_{fbF}+\phi_{nt}-\phi_{Sx})^2-\left(V_{GF}-V_{fbB}+\phi_{nt}-\phi_{Sx}+\frac{qN_{ch}t_{Si}^2}{\varepsilon_{Si}}\right)^2\right]-\frac{qN_{ch}t_{Si}^2}{\varepsilon_{Si}}\right\}, \tag{22}$$

$$I_{S1}=e^{-(2\phi_{fx}+bV_{DS})/V_T}\left(1-\exp\left(-\frac{q\,N_{ch}\,t_{Si}^2}{V_T\,\varepsilon_{Si}}\right)\right), \tag{23}$$

$$I_{S2}=1-\exp\left(\frac{q\,N_{ch}\,t_{Si}^2}{V_T\,\varepsilon_{Si}}\right). \tag{24}$$

The surface potential ϕ_S from the diode circuit in Fig. 7 represents the equation solution (21) for any combination of voltage variables V_{DS} and V_{GS}.

5. Simulation Results and Discussion

The ionizing radiation has the effects on the changes of the electric characteristics of the transistor. In the paper, the approaches described in the Section 3 are used for the simulation of electric characteristics of the transistor and the results are compared with numerical results.

5.1. Modeling of N_{ox} and D_{it} effects in MOS transistor

Including of the effects N_{ox} and D_{it} in the NQS MOS transistor model is made by incorporation of the correctional potential ϕ_{nt} in the surface potential equation (eqn. 20). As already stated, with diode circuits as in Fig. 4, by using mathematical apparatus available in the Spice, the boundary surface potentials are acquired, and based on them the equivalent line is solved (Fig. 3). In this paper, the equivalent line is divided on 10 equal segments. Fig. 8 shows the acquired surface potentials that show the impact of N_{ox} (Fig. 8(a)) and the impact of the interface trapped charges through D_{it} on the surface potential value. The results acquired with diode circuits are shown with solid line, while the numerical results are shown with open circles. A solid compliance of the results confirms the efficiency of the diode circuit as a new method for solving iterative relations (21). As it can be seen on the figure, the surface potential is changed for constant negative voltage shift with the increase of N_{ox}, while $D_{it} = 0$. In the case of the increase of D_{it} while $N_{ox} = 0$, the voltage shift of the surface potential will depend on its value due to the dynamic charge contribution on SiO_2-Si interface. Namely, the interface charges have the energy inside forbidden zone. Interface trapped charges with energies above intrinsic energy level E_i behave as acceptor-like charges, while all interface trapped charges with energies below intrinsic energy level behave as donor-like charges, which is experimentally verified [2,30,31].

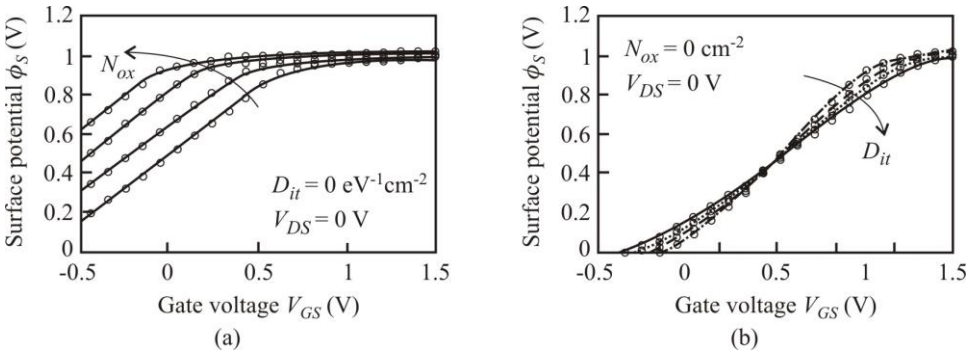

Fig. 8 Surface potential versus gate voltage dependence for different values of N_{ox} at $D_{it} = 0$ (a) and for different values of D_{it} at $N_{ox} = 0$ (b) obtained from Spice simalation of proposed model (solid line) and TCAD numerical results (open circles) for MOS transistor with $t_{ox} = 5$ nm and $N_{ch} = 4 \cdot 10^{17}$ cm^{-3}

Fig. 9 shows the transfer characteristics of MOS obtained from the Spice and compared with TCAD numerical results, which shows solid compliance of the results of the applied method in NQS MOS model with the TCAD numerical results.

It is important to state that in [2] is used the same expression for correctional potential due to the effects of ionizing radiation, by using voltage-controlled voltage source (VCVS) with voltage:

$$V_{DF} = f(V_{GB}, V_{SB}, N_{ox}, D_{it}) = f(\phi_S) \tag{25}$$

and which is series connected to transistor gate, for which some of standard models are used (for example, BSIM model). For determining $V_{DF} = \phi_{nT}$, respectively solving (19) the authors used the non-iterative algorithm inside the Verilog-A model [2], while in our method the iterative equation for determining the surface potential was solved in a physical way, with diode subcircuits.

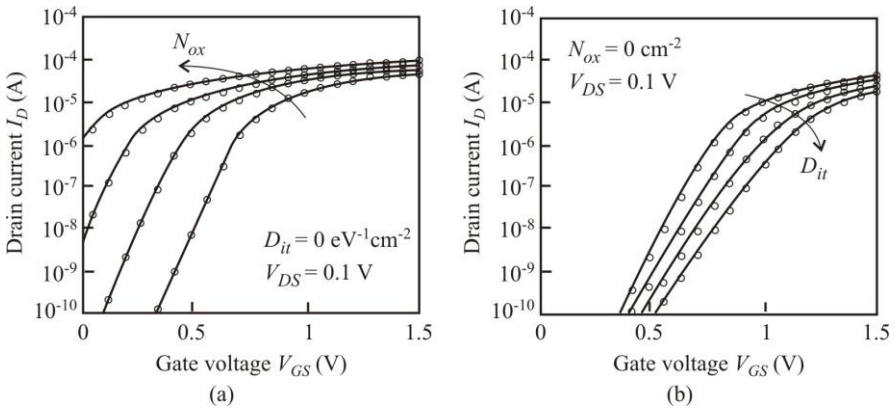

Fig. 9 Transfer characteristics $I_D(V_{GS})$ for different values of N_{ox} at D_{it} = 0 (a) and for different values of D_{it} at N_{ox} = 0 (b) obtained from Spice simalation of proposed model (solid line) and TCAD numerical results (open circles)

5.2. Modeling of N_{ox} and D_{it} effects in FinFET

With the scaling of the device dimensions, conventional transistors reached its limits, so new technological structures for future generations of integrated circuits are emerging. Such structure is fully-depleted floating-body (fin) multi-gate FET (FinFET) [32]. However, recently it has been shown that FinFET technology has rapid rate of aging, so that the degradation on FinFET exceeds the degradation of the planar technology node by higher stress voltage and longer time [33]. Therefore, the modelling of ionizing radiation effects in these structures is important. In the standard BSIM.CMG model [34] for FinFET, however, there is only fitting parameter CIT (interface trap capacitance parameter) in sub-threshold region [35], while it does not have a possibility for user-defined input of oxide trapped charges.

Fig. 10 shows a schematic presentation of n-type FinFET analysed in this paper (with the following parameters L = 0.9 μm, t_{ox} = 5 nm, t_{Si} = 20 nm, $N_{ch} = 2.4 \cdot 10^{18}$ cm^{-3} and $N_D = 10^{20}$ cm^{-3}).

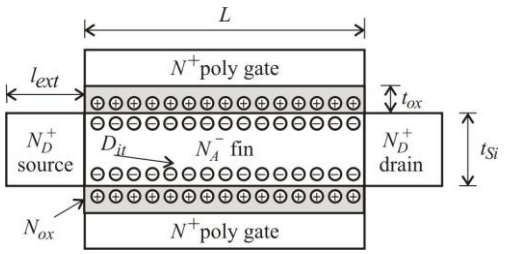

Fig. 10 Schematic representation of n-type FinFET

Fig. 11 shows the output characteristics of transistor obtained by using TCAD numerical results, BSIM.CMG model which parameters are acquired by fitting, and modified NQS SOI model. In order to simplify the tuning of the parameters of BSIM.CMG model, a simulate structure has a long channel and the thickness of oxide gate and silicon fin, so the effects of a short channel can be neglected, and the silicon fin is fully depleted [28,36]. The same parameter set is used for p-type FinFET, with the fact that the fin film has the opposite doping (n-type fin film). In the absence of the ionizing radiation effects, the compliance of results of different models is shown [28].

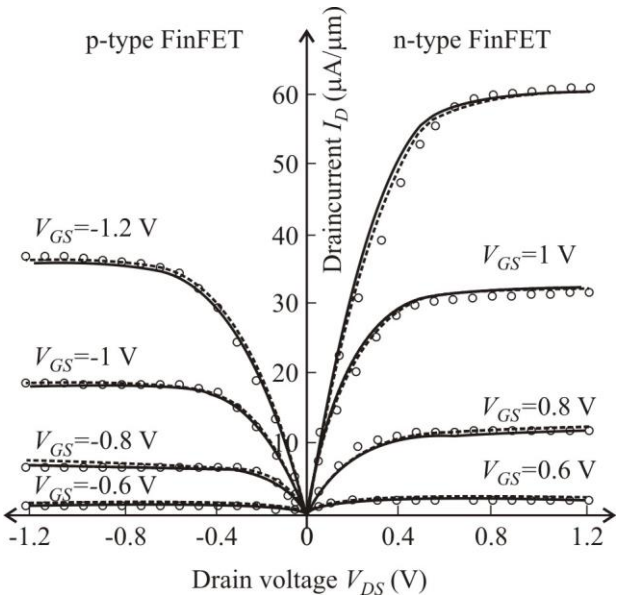

Fig. 11 The output characteristics of n and p-type FinFETs simulated for N_{ox} = 0 and D_{it} = 0 with Spice using BSIM.CMG model (solid line), NQS SOI model (dashed line) and TCAD simulator Silvaco Atlas (open circles)

Modeling of N_{ox} and D_{it} effects by using auxiliary diode subcircuits (ADS) for solving surface potential equations (21) is possible in two ways: by using NQS SOI model (time consuming), or as shown in [2,6], for determining surface potential as control voltage of VCVS for producing $V_{DF} = \phi_{nt} = f(V_{GB}, V_{SB}, N_{ox}, D_{it})$. This VCVS is connected in series with gate node of BSIM.CMG model, as shown in Fig. 12.

Second approach of modelling the ionizing radiation effects in FinFET is at time more comfortable, because the simulation execution time is shorter and there are no problems due to convergence, but due to a physical dependency the NQS SOI model is more convenient, because other effects important for the operation of FINFET can be easily included (for example, quantum-mechanic effects). The second approach, BSIM.CMG model with ADS, was used in this paper for modelling the ionizing radiation effects.

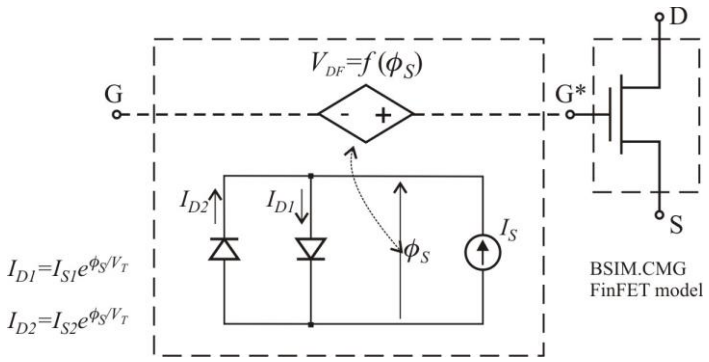

Fig. 12 Schematic of diode subcircuit shown together with the BSIM.CMG FinFET model as implemented in Spice simulations to include the effects of N_{ox} and D_{it}

Fig. 13 shows transfer characteristics of n and p-type FinFETs for different values of D_{it} while N_{ox} = 0. Fig. 14 shows transfer characteristics for different values of N_{ox} while D_{it} = 0, and Fig. 15 shows characteristics for combinations of different values of N_{ox} and D_{it}. In Figs. 14 and 15 there are no results obtained by BSIM.CMG model because oxide trapped charge effect is not included in this model. All characteristics are generated for V_{DS} = 1.2V. In the BSIM.CMG model, a parameter CIT is determined for given D_{it}. Parameter b, which appears in the equation (21), was used with value b = 0.05, for the reason previously explained in Section 4. All stated characteristics show good match of suggested approaches with TCAD numerical results [28,37].

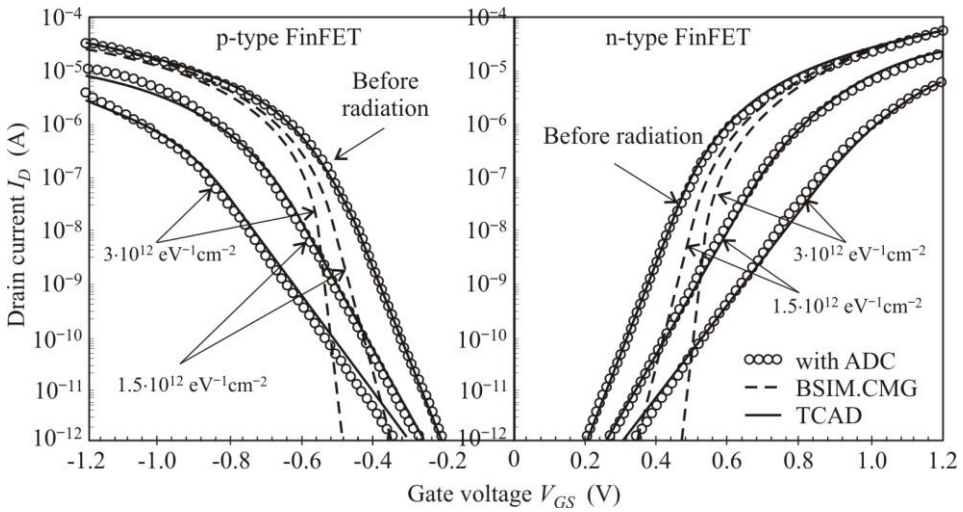

Fig. 13 Transfer characteristics $I_D(V_{GS})$ for different values of D_{it} at N_{ox} = 0

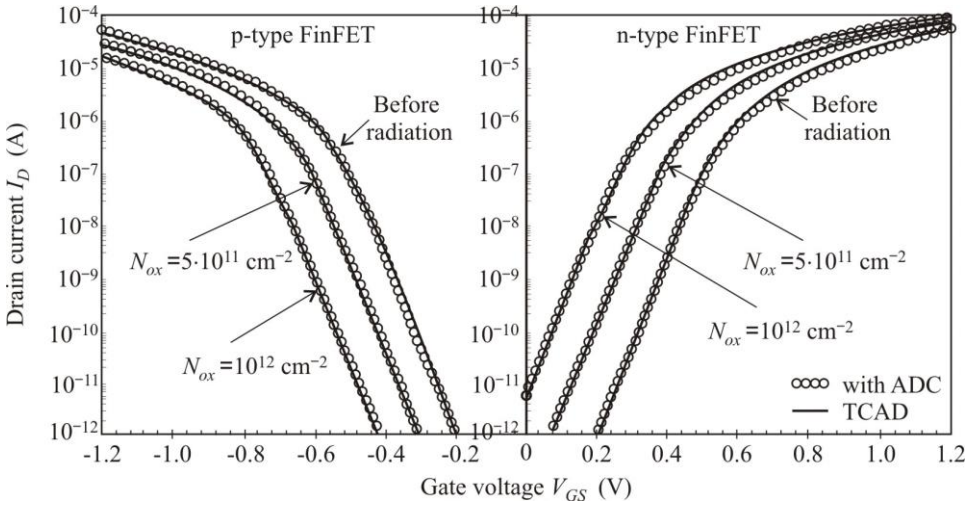

Fig. 14 Transfer characteristics $I_D(V_{GS})$ for different values of N_{ox} at D_{it} = 0

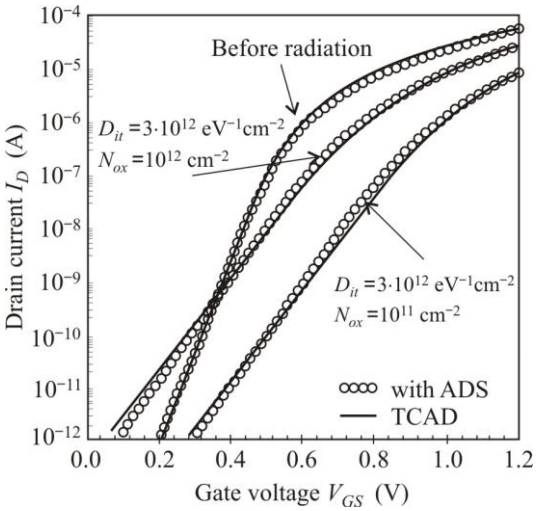

Fig. 15 Transfer characteristics $I_D(V_{GS})$ for combined influence of N_{ox} and D_{it} for n-type FinFET

Fig. 16 shows changes of threshold voltages for n and p-type FinFETs after ionizing radiation, obtained from TCAD and proposed method. The constant current method is used for threshold voltage extraction [28,38], with I_D' = 100 nA/μm. The impact of this ionizing radiation effect is also experimentally confirmed [39].

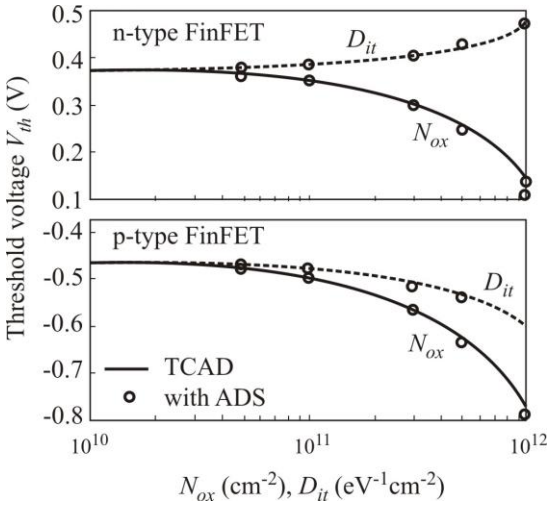

Fig. 16 Theshold voltages V_{th} for p and n-type FinFET as function of N_{ox} and D_{it}.

6. CONCLUSION

The modelling of ionizing radiation effects for CMOS devices is presented in this paper. It is shown how surface potential equations can be modified with correctional potential, which is a result of existence of oxide charges and interface trapped charges. Auxiliary diode circuits were used for determining modified surface potentials, while for obtaining electric characteristics of devices, two approaches were used, previously developed non-stationary models for CMOS devices and, second approach, VCVS (with controlled voltage obtained by diode circuits) in series with gate node of standard models. In comparison with TCAD numerical simulations, the efficiency of suggested approaches for prediction of impacts of dynamic effects of both oxide and interface trapped charges on electrical characteristics of devices is shown.

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